Self-Initializing Memory Elements

Bapiraju Vinnakota, Member, IEEE and Ramesh Harjani, Member, IEEE

Abstract—Test generation for sequential circuits is complicated by the fact that the initial internal state of a circuit, after power-up, cannot be predicted. This is commonly referred to as the initializability problem. In this paper, we present a new solution to the initialization problem—self-initializing memory elements (SIME's). SIME's are designed to initialize, at power-up, to a known state. The start-up environment of a memory element is analyzed in detail. This analysis is used to design several different types of SIME's. Each of the designs meet different user requirements. We also discuss the application of SIME's to the problem of test generation for sequential circuits. SIME's have distinct advantages over on-chip reset signals. Compared to off-chip reset signals, they offer a different overhead-benefit trade-off. They may also be used in conjunction with other design for test techniques. In short, they provide a designer with additional flexibility during the design process.

I. INTRODUCTION

SEQUENTIAL logic circuits possess memory elements (ME's), which store the internal state of the circuit. The outputs produced by such circuits are influenced by the inputs as well as the internal state. Normally, in a sequential circuit, the initial state at power-up is not predictable. Consequently, the input/output relationship immediately after power-up is also not predictable. In many applications, this is not satisfactory. Sequential circuit testing [1]–[4] is an application where knowledge of the initial state is beneficial. Possessing knowledge of the state of a circuit prior to test application can greatly reduce the cost of testing. This problem is often referred to as the initializability problem for sequential logic circuits [4], [5]. Several test generation algorithms that do not depend on knowledge of the initial state [1], [2], [9] have been proposed. Other solutions are based on information derived from the functional representation of the circuit under test (CUT) [10], [11]. Design for testability techniques [4] are also used to deal with the problem. Each solution to the initializability problem incurs a cost in terms of area, performance, the ease of test generation, and test set quality.

We propose a new solution to the initializability problem: self-initializing memory elements (SIME's). A SIME is designed to initialize to a known state (of the users choice) on circuit power-up. While on-chip reset signals have been proposed by others, we believe SIME's have significant advantages over on-chip reset signals. The rest of this paper is organized as follows: Previous work related to the initializability problem is reviewed briefly in Section II. In Section III, we describe the design and analysis of SIME's. In Section IV, we discuss the use of SIME's in test generation for sequential circuits. We conclude in Section V with a summary of our results.

II. PREVIOUS WORK

Test pattern generation (TPG) algorithms that do not require any knowledge of the initial state [1], [2], [9] are one solution to the initializability problem. Usually, the computational effort involved in generating a test set using these algorithms is significantly higher compared to test generation algorithms [3] which rely on knowledge of the state of the CUT. Additionally, the fault coverages obtained by such algorithms may be lower, and the test sets generated may also be larger. Thus, possessing knowledge of the initial state prior to test application is beneficial. Some TPG algorithms attempt to bring the CUT to a particular known state, irrespective of the power-up state, through the use of an initialization sequence [7], [8]. Unfortunately, test generators are often unable to derive initialization sequences for many circuits. Extensive fault simulation may also be required to predict the behavior of the initialization sequence in faulty circuits. Cheng and Agrawal [5] suggest altering the state assignment process to design easily initializable circuits. Their approach is based on the use of synchronizing sequences. To generate these sequences, it is necessary to possess a functional description of the sequential logic circuit being synthesized. These descriptions are not always available. Second, not all FSM's possess synchronizing sequences.

One popular solution is the use of a reset signal [4]. Here, the reset and/or clear inputs of all the ME's on the IC are wired together. This global wire is then connected to an input pin. Exercising the reset signal initializes the sequential logic circuit to a known state asynchronously. Several different types of configurations [4] are possible for global reset/clear signals. The main advantage of a reset signal is its simplicity. However, there are two drawbacks. The first is that an extra input pin is required for the reset signal. This may be a problem in some applications. Second, a significant overhead is incurred in routing the reset signal globally. On-chip reset signals [4], [12] address only the first of these drawbacks by moving initialization circuitry on to the IC. In both cases (but especially with an on-chip reset) the effect of a single stuck-at fault on the initialization capability cannot be predicted easily. A single fault may affect the ability to initialize a single ME, several ME's, or all the ME's in the IC. Scan design techniques [4], [13] are an alternative to the reset signal. In a simple scan design, all the ME's on the chip are linked to form a shift register. The problem of sequential test generation is reduced to combinational circuit test generation. However, there is a significant area and performance penalty associated with scan

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The authors are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 USA.

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Fig. 1. Two common ME designs.

III. CIRCUIT DESIGN

Before we discuss various transistor-level circuit designs for SIME’s, we analyze the start-up transient environment in a normal ME. We present a model for a regular noninitializing ME and discuss some system level constraints including noise and start-up behavior. Finally, we describe different transistor-level circuit realizations for the SIME and discuss their system-level implications.

SIME Model

Fig. 1 shows two variations for regular (nonself-initializing) ME’s used commonly in sequential design. The design in Fig. 1(a) uses only one CMOS switch to load data into the ME. The data is stored automatically, using regeneration from \( \text{Inv}_2 \). The circuit in Fig. 1(b), however, uses two CMOS switches. One is used to load data, and the second is used to store data. The store switch is turned on as soon as the loading operation is complete.

During the start-up transient, no assumptions about the load switch or the input data value can be made. Hence, it is necessary to accomplish two independent functions in designing a SIME. First, it is necessary to initialize the ME to a known state. Second, since the start-up transient behavior of the input cannot be predicted, it is necessary to isolate the ME from the rest of the system until the overall system has settled to a quiescent state. The time taken to settle to a quiescent state is application dependent. It is possible to develop SIME’s for both variations of ME’s shown in Fig. 1. However, because of its regeneration properties, we use the circuit in Fig. 1(a) for our SIME designs.

A block diagram view of the SIME design is shown in Fig. 2. As mentioned earlier, this circuit has two additional blocks, an isolation block and an initialization block. During start-up, the primary purpose of the isolation block is to ensure that spurious data at the input does not delete the initialized value of the ME. Clearly, if the SIME is being initialized to a zero, then it is only necessary to block the ones coming through. Likewise, if the SIME is being initialized to a one, then only zeros need to be blocked. Fig. 3 shows the isolation circuit used to prevent ones from passing through. This circuit initializes to a zero (SIME 0). In this circuit, when isolate is low transistor, \( IS_2 \) is off, and even if both the load and data input lines are high, node 4 will not be pulled down. A low data with load enabled would turn transistor \( IS_3 \) on, but this does not pose any problem because node 4 is already being initialized high via transistor \( IN_1 \). Initialization occurs by maintaining initialize low during the power-up period. During normal operation, isolate is high, and transistor \( IS_2 \) is completely on. Hence, the isolation block is effectively an inverter. To maintain correct data polarity, the output connection is moved to the left of the last inverter as shown in Fig. 3. From a theoretical perspective, the initialization and isolation signals can be generated independently. However, since initialization occurs fairly rapidly, it is counterproductive to operate the initialization signal for a period longer than the isolation signal. Hence, generating the signals from one source is a more economical solution. If we tie the two signals together, then transistors \( IS_1, IS_2, IS_3 \), and \( IN_1 \) form a NAND gate. We refer to the entire initializing and isolating circuitry as the I/I block. In a similar fashion, a zero isolating circuit can be constructed, as shown in Fig. 4. If we wish to use the SIME to initialize to a one. Here one, a SIME initializing to state 1(0) will be called a SIME 1 (SIME 0). The I/I block for it would use a NOR gate rather than a NAND gate and the isolate/initialize signal would have to be maintained high during start-up and low during normal operation. There are a number of circuit implementations possible to generate the necessary initialization and isolation signal. But first, it is necessary to understand the start-up behavior of the memory cell itself.

Start-Up Behavior: Fig. 5 shows a transistor-level circuit diagram for a ME [20]. Transistors \( Q_1 \) and \( Q_5 \) form one inverter, and transistors \( Q_2 \) and \( Q_4 \) form the other. We shall first assume a steady-state supply voltage and analyze the ME in isolation. The memory cell has two stable states \( (0,1) \) and a quasistable state somewhere in between. The
the ME from the rest of the circuit. We shall also assume that the initialization stage is totally disconnected. To simplify things further, we shall assume complete symmetry, i.e., transistor \( Q_1 \) is identical to \( Q_2 \), and transistor \( Q_3 \) is identical to \( Q_4 \). For a fixed value of \( V_{DD} \) and zero voltage difference between the voltages at nodes A and B, all the transistors are operating in the saturation region. A small-signal model for the ME can then be derived as shown in Fig. 6. In this figure, \( g_m = g_{ds1} + g_{ds3} \) represents the small-signal conductance from node A to ground, \( c_A \approx c_{gs1} + c_{gs3} \) represents the capacitive load at node A, \( g_{m4} = g_{m2} + g_{m4} \) is the sum of the transconductances of transistors \( Q_2 \) and \( Q_4 \). Likewise, \( g_b = g_{ds2} + g_{ds4} \) represents the small-signal conductance from node B to ground, \( c_B \approx c_{gs2} + c_{gs4} \) represents the capacitive load at node B, \( g_{m6} = g_{m1} + g_{m3} \) is the sum of the transconductances of transistors \( Q_1 \) and \( Q_3 \). In this figure, \( I_{OFF} \) describes the asymmetrical noise current entering node A during the start-up transient. Any symmetrical current entering both nodes A and B does not cause any change in the voltage difference between the nodes A and B and can therefore be neglected for this analysis.

Assuming complete symmetry and also assuming that \( g_m \) is much larger than \( g_{ds} \) (\( g_m/g_{ds} \gg 1 \)), the time-domain response for the ME output voltage is approximately given by (1). In this equation, \( g_m = g_{m3} = g_{m4} \), \( c_A \approx c_B \approx c \), and \( V_{ab}(t) \) is the difference in the voltages at node A and node B at time equal to zero. For the case when \( I_{OFF} \) is equal to zero, and \( V_{ab}(t) \) is nonzero, the output voltage rapidly goes to the rails

\[
V_{ab(t)} = \frac{I_{ON}}{g_m} + \frac{1}{2} \left( \frac{I_{OFF}}{g_m} - V_{ab(0)} \right) e^{\frac{-c}{t}} + \frac{c}{t}.
\]

(1)

For any value of supply voltage, only the difference in voltages at nodes A and B is amplified. In the ideal case with no device noise, the ME will start up at the symmetrical meta-stable state. It cannot start up in either logic state as that would imply an asymmetry in the design. The voltages at node A and B at this point is equal to the logic threshold of the two inverters formed by \( Q_1, Q_2 \) and \( Q_3, Q_4 \). However, due to noise there is likely to be a little asymmetry between the starting voltages at nodes A and B. This difference is amplified by the positive feedback of the memory cell and quickly results in either a 1 or 0 being stored in the cell.

We shall revisit the memory cell transient response with the power supply not at a steady state and will also discuss
noise issues. However, before we do so we shall first consider a model for the power supply during the start-up transient. Fig. 7 shows a model for the start-up transient of a typical power supply. There is an initial start-up ramp followed by normal operation. The overshoot period is neglected for our analysis because the decision to start up at a 1 or a 0 state is usually made long before the supply voltage reaches the normal operating voltage. The rate of change of the supply voltage during this period can vary dramatically and depends on a combination of the capacitive and resistive loads at the output of the power supply and the output impedance of the regulated power supply. For our purposes, we shall assume the use of a regulated power supply. This limits the overshoot and therefore further validates our simple ramp assumption.

**Noise Model**

During the start-up transient, the ME is also subjected to noise from the transistors. An accurate noise model that includes all the various forms of noise is extremely difficult to develop. This is particularly true during the ramp phase where the transistors travel through different operating regions. However, the analysis below derives a noise model that provides a good estimate of the noise. The effects of all the noise sources are simulated by using a single equivalent noise current, \( I_{1N} \), incident at one of the two output nodes of the ME.

\[
R_T^2 = \left[ \frac{8kTg_m(1+\eta)}{3} + \frac{K_{FD}}{f_{CO}W L} \right] \Delta f. \tag{2}
\]

During the early part of the start-up ramp, when \( V_{DD} \leq |V_{ON,MAX}| + |V_{ON,MIN}| \) the transistors operate in weak or moderate inversion and for supply voltages greater than this value, they operate in strong inversion. So, we need to consider the effects of noise in both the strong and weak inversion regions. Equation (2) describes a strong inversion thermal and flicker noise model for a MOS transistor operating in saturation. The model for noise in weak inversion can be described similarly [17]–[19]. Only the flicker and thermal terms need to be modified to include the plateau in \( R_T^2 \) in weak inversion. To calculate the effective rms noise current, we need to integrate (2) from \( f_{min} \) to \( f_{max} \). Where \( f_{min} \) and \( f_{max} \) are the minimum and maximum frequencies of interest.

\[
\frac{V_a}{I_{1N}} = \frac{K_{e} \left( S + \frac{g_m}{c} \right)}{\left( S - \frac{g_m}{c} \right) \left( S - \frac{g_m}{c} \right)} \tag{3}
\]

The value for the \( f_{max} \) can be calculated from the frequency domain transfer function for the ME shown in (3). The system has one zero and two poles, however, there is significant pole-zero cancellation at high-frequencies, and the system can be treated as single pole system. Using (3), it is possible to show that the 3 dB bandwidth seen by the current noise source \( I_{1N} \) is given by (4). As mentioned earlier \( g_m \) is the conductance of the transistors, \( gds \) is the output conductance, and \( c \) is the load capacitance at the output nodes of the ME. To the first order, in strong inversion, the 3 dB frequency is independent of supply current, and for weak inversion, it increases linearly with increased supply current. The upper integration limit \( f_{max} \) in our integration for the effective rms noise current can now be set to \( (\pi/2)f_{3dB} \), [22]

\[
f_{3dB} = \frac{1}{\pi} \left( \frac{g_m}{gds} \right) \frac{g_m}{c}. \tag{4}
\]

The minimum frequency of interest \( f_{min} \) is important when considering the flicker noise component. During the input supply voltage ramp at any time point \( t \), the minimum frequency possible is equal to \( 1/(t - t_0) \) — see Fig. 7. Therefore, for any time \( t \) in the ramp, we can use a new value of \( f_{min} \) and perform an integration of our noise model. The lower integration limit \( f_{min} \) would vary from \( f_{min} = 1/(t_{max} - t_0) \) to \( f_{min} = f_{max} \). Under most circumstances, the final outcome of the ME is usually decided substantially earlier than time \( t_{max} \), however, the exact time when a decision is made is highly unpredictable and depends on the magnitude of the noise current. Also note that as the slope of input ramp increases so does \( f_{min} \).

Using the analysis just mentioned and also considering the regions of operation of the devices, we can calculate the total rms noise current \( I_{1N} \) at any time \( t \). At \( t \) equal to \( t_0 \), the supply voltage is zero and increases linearly until \( t = t_0 + \text{risetime} \) the supply voltage reaches \( V_{DD,max} \). For our analysis, we use \( V_{DD,max} = 5.0 \), and the \( \text{risetime} \) was varied from 1 \( \mu S \) to 24 hours. In Fig. 8, we plot the total rms noise current \( I_{1N} \) versus \( V_{DD} \) for \( \text{risetimes} \) equal to 1 \( \mu S \) and 1 S. Here, we make the assumption that the ME is in the meta-stable state throughout the supply range. In the actual circuit, the noise current is a function of the drain-to-source currents through the transistors and goes to zero when the memory cell reaches a valid logic level, i.e., the voltages at nodes A and B go to \( V_{DD} \) or \( V_{SS} \). We use the relationship between the device current and noise current in our SPICE simulations to reflect real world effects. Using the same calculations and the relationship between the supply current and \( V_{DD} \), in Fig. 9, we plot \( I_{1N} \) versus \( I_{DD} \) for \( \text{risetimes} \) equal to 1 \( \mu S \) and 1 S. It is clear from this figure that the risetime of the supply ramp does not have any significant effect on the noise current. The approximate doubling in the noise current we see in Fig. 9 results from a variation in the risetime by six orders of magnitude. This relationship between the \( I_{1N} \) and \( I_{DD} \) is used in SPICE with help of the current-controlled-current-sources (CCCS’s) and look-up tables to simulate the effect of circuit noise on the memory cell during start-up.
Isolation/Initialization

We have just described the environment that a memory cell is likely to see during start-up. Previously, we discussed how a SIME might be designed. However, we did not describe how the isolate/initialize signal is generated. The primary interest during the design of the initialization circuit is to guarantee that the cell will power up to a known state. And the primary purpose of the isolation circuit is to guarantee that a spurious signal at the input does not affect the initialization. Our goals are to design circuits that have minimal impact during normal operation and low power and area overheads. We will present three designs to generate the I/I signal. All the designs are based on delaying the voltage at the isolate/initialize node in Fig. 3. (This circuit is designed to initialize a SIME to state 0.)

All the circuits use an initialization transistor and an isolation transistor. The gate voltages for these transistors are controlled by a capacitor and a charging system. A conceptual view of this circuit is shown in Fig. 10. Only the initialization transistor is shown in this figure. The gate of the isolation transistor IS2, shown in Fig. 3 is also tied to node VS. A capacitor is tied from the node VS to VSS, and the voltage on this node is kept low for a period of time. After a predetermined period of time, the voltage at this node is charged to VDD such that the initialization transistor IN1 (PMOS, in this case) is completely turned off, and the isolation transistor is totally turned on. (The circuit to initialize a SIME to 1 would use an NMOS transistor for IN1, the capacitor, CINIT would be connected between node VS and VDD, and the charging circuit would be connected between VS and VSS.) Traditionally, a reset transistor in a memory cell accomplishes the same function as our initialization transistor. We shall use the terms initialization
transistor and reset transistor interchangeably. A number of different circuit implementations are possible for the charging circuit, and the design of a compact capacitance also requires some consideration. To illustrate the interaction between the capacitance and the charging circuit, we shall describe a complete example of an initialization circuit using the delayed start-up technique. We shall subsequently describe the other circuit implementations and their design trade-offs.

Before we describe the initialization circuit, we shall briefly examine the isolation circuit. The isolation process can best be understood by examining Fig. 3 and Fig. 5. As we will soon see, initialization occurs fairly rapidly, usually before the supply voltage is equal to the threshold voltage of the NMOS transistors. Therefore, we can safely assume that the initialization value is set when we evaluate the isolation circuit. If we assume the worst case scenario, i.e., due to spurious signals at start-up, both DataIN and Load are high. Then, we can calculate the maximum voltage allowed at node isolate/initialize that would still ensure isolation. Because initialization is complete, node B is low, and transistor Q3 is completely turned on. Transistor Q2 is completely off and only the gates of transistors Q3 and Q4 are tied to node A and do not affect the current equations. In addition, because the input is assumed to be high, assuming worst case scenario, transistor IS1 is completely on, and transistor IS3 is completely off. Using Kirchhoff’s current law, the current flowing through transistor IS2 (which is equal to current through transistor IS1) is equal to sum of the currents through transistors IN1 and Q3. Isolation can be guaranteed as long as the voltage at node A is less than the logic threshold voltage of the inverter formed by transistors Q3 and Q4. When the voltage at node A is equal to the logic threshold, the voltage transistor IS3 is in the saturation region, and transistor Q3 is in the linear region. Summing the currents and equating it to zero, we get

$$0 = \frac{k_p}{2} W_{Q3} \left( \frac{V_{DD} + V_T}{2} - \frac{V_{logic}}{2} \right) \left( \frac{V_{DD} - V_{logic}}{2} \right) - \frac{k_n}{2} W_{IS2} (V_S - V_T)^2 + \frac{k_p}{2} W_{IN1} (V_{DD} - V_x + V_T)^2. \quad (5)$$

We can now calculate the maximum voltage, $V_{\text{max}}$, at the isolate/initialize node that still ensures that the voltage at node A is less than the logic threshold voltage. Isolation is guaranteed for all voltages less than $V_{\text{max}}$. Symbolic calculation for $V_{\text{max}}$, results in a quadratic expression that is fairly complex. However, the value for $V_{\text{max}}$ can be evaluated numerically fairly easily. In our example, we have used unit-sized transistors, except for transistors IS1 and IN1, which are three times as wide, and calculated this voltage. SPICE simulation was used to validate our calculations. As seen in Fig. 11, SPICE gives us a value of 3.63 V for $V_{\text{max}}$, and our calculations suggest a value of 3.584 V. This result is extremely close when you consider that our calculations do not account for numerous second-order effects. In addition, this calculation assumes that the drain-to-source voltage of transistor IS1 is zero. When the input is high, transistor IS1 is in the triode region and effectively acts as a nonlinear resistance. If we include the negative feedback provided by this resistance, then $V_{\text{max}}$ increases to approximately 4.0 V. The addition of this nonlinear term makes a closed-form solution impossible, and only a numerical solution is possible. It is also important to note that this voltage is much higher than the nominal logic threshold voltage, which for our example design is 2.1 V. This voltage is also much higher than the threshold voltage of the NMOS transistors, which ensures that initialization is complete long before isolation cannot be guaranteed. Additionally, the time it takes to reach $V_{\text{max}}$ sets a maximum bound on the settling time for the signals entering the ME.

We next describe the circuits used to keep the voltage at $V_x$ low. As mentioned earlier, both isolation and initialization is guaranteed by keeping this voltage low for a sufficient period. 

**Active RC Delay Start-up:** This circuit realizes the required delay using an RC circuit. An RC delay start-up is envisioned...
in [4], but no specific implementation is discussed. We do so here. In the design shown in Fig. 12, transistor Q5 is the initialization transistor. The gate-to-source and gate-to-bulk capacitances of transistor Q6 are used to provide a low area overhead capacitance $C_{Q5}$ from node $V_x$ to ground. Using the gate capacitance of a transistor provides the smallest silicon area capacitance on an integrated circuit. During normal use, this capacitance is highly nonlinear. However, for our purposes, the linearity of the capacitance is of little importance. Transistor $Q7$ turns on when $V_{DD}$ is greater than $|V_{TH}|$ and acts as a nonlinear resistor. When the supply voltage is less than $|V_{TH}|$, the transistor is essentially off or operating in weak inversion. So, at the start of the supply voltage transient, the voltage at node $V_x$ is equal to zero. However, as the supply voltage increases, the gate-to-source voltage for $Q7$ becomes increasingly larger, and the transistor is turned on charging up the gate capacitance $C_{Q5}$ to $V_{DD}$.

During normal operation, without the initialization circuit, the voltages at node A and node B increase equally with increased supply voltage. They are approximately somewhere halfway between $V_{DD}$ and ground, and the actual value depends on the capacitive and voltage division. Fig. 13 shows the value of this voltage for different values of supply voltage. We have disconnected the loop to remove the effect of regeneration for this simulation. We note two things, 1) both the node voltages are equal and, 2) the memory cell remains in the meta-stable state for this completely symmetrical case.

At the start of the supply transient, the voltage at node $V_x$ is low, near ground, and then slowly follows the supply voltage. However, there is a possibility that there might be some residual charge left over from the previous $ON$ period. For our circuit to function correctly, it is not essential that the starting voltage at node $V_x$ be identical to zero. However, it is reasonable to expect that the charge stored on capacitors from a previous $ON$ period will rapidly decay to zero because of partially forward-biased PN junctions and other leakage currents. Therefore, if any charge is retained at all, it is not likely to be large. After power-down, where node $V_{SS} = V_{DD} = 0$, the largest voltage possible across any capacitance within the entire chip is approximately 0.7 V. Furthermore, the reverse leakage currents of PN junctions will rapidly discharge any stored voltages in a few hundredths of a second. Therefore, our assumption of 0 V across is valid for both cold and warm starts. Because the start-up voltage at node $V_x$ is near zero, transistor $Q5$ is turned $ON$ and pulls up the voltage at node B to $V_{DD}$. As the supply voltage increases both the node voltages

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**Fig. 13.** SPICE simulation showing meta-stable state.

**Fig. 14.** SPICE simulation showing the effect of RC delay reset action.

**Fig. 15.** Reset circuit with device parasitics.
increase. However, the voltage at node B rises more rapidly and follows $V_{DD}$, while the voltage at node A does not rise as rapidly. The positive feedback of the memory cell further amplifies this difference between the two node voltages, and the voltage at node A goes to ground, while that at node B follows $V_{DD}$. A simulation of this effect, without any noise current, is shown in Fig. 14. Note that the decision to be a one or a zero is made extremely early, $V_{DD}<0.5$ V.

Clearly, when the ME is used as an ideal one, the RC delay circuit correctly initializes the circuit. However, if initialization is to be guaranteed, a more careful study of the reset circuit is necessary. Fig. 15 shows the reset circuit with some parasitic device capacitances shown. In this figure, $C_{BvDD}$ is the capacitance from node B to $V_{DD}$, $C_{BQ0}$ is the capacitance from node B to ground, $C_{BQ2}$ is the gate capacitance of transistor Q2, and $C_{BQ3}$ is the gate capacitance of transistor Q3. During the supply voltage ramp, the node voltage $V_{z}$ is not zero but is equal to $V_{z} = \frac{C_{BQ2}}{C_{BQ2} + C_{BQ3}} V_{DD}$ because of the constant rate of change of $V_{DD}$. If we are to keep transistor Q2 ON, then $V_{z}$ has to be made small, which in turn implies that $C_{BQ0}$ should be much smaller than $C_{Q6}$. The reset transistor Q5 can be made small, unit sized, and the gate area of Q6 should be made approximately ten times larger. Transistor Q7 acts as a resistor. To keep the voltage at node $V_{z}$ low for any appreciable time, the $W/L$ ratio of Q7 should be kept small to increase the resistance. Fig. 16 shows the results from simulation of the final design. This simulation includes the effects of circuit noise. We see that the voltage at node B follows the supply, and the voltage at node A rapidly goes to zero. This is exactly the initialization we wish to accomplish.

The design of Fig. 12 constrains the risetime of $V_{DD}$. We assumed that the active resistance transistor ($Q_7$ in Fig. 12) only turned on when the supply voltage was greater than $|V_{T_T}|$. This assumption is fairly accurate for short supply voltage start-up ramps. However, for very long start-up times, the subthreshold current of $Q_7$ slowly charges up $V_{z}$ such that it follows the supply voltage. If this happens, initialization will fail. The active RC delay circuit works fairly well for supply voltage start-up times in the range of a few to tens of microseconds. Because of the characteristics of noise and the many circuit nonlinearities, a closed-form solution for the initialization time is not possible. However, once we calculate $V_{zmax}$, then a closed-form solution for the isolation time for extremely fast supply voltage start-up times can be provided and is given by

$$
T_{iso} = \frac{V_{T_T} C_{init}}{2} \left( \frac{V_{dd} + V_{T_T}}{V_{dd}} \right)^2 \ln \left[ \frac{V_{zmax}}{V_{T_T}} \left( \frac{V_{dd} + \frac{3}{2} V_{T_T}}{V_{dd} + V_{T_T}} - \frac{1}{2} V_{zmax} \right) \right].
$$

The isolation and initialization times period provided by this circuit is of the order of microseconds. A longer isolation time may be desirable for some applications. The following designs are aimed at addressing this problem.

Leakage Current Delayed Start-up: The second circuit implementation for the delayed start-up is shown in Fig. 17. In this circuit, the charging current is provided by the reverse leakage current of drain-to-bulk or source-to-bulk junction diodes as shown in the figure. The magnitude of the charging
current can be varied by altering the perimeter and area of the drain or source diodes. This circuit is capable of providing a large range of delay times, all the way from a hundred microseconds to a few seconds. Correspondingly, this design is capable of isolating the SIME for a similar time period.

However, reverse leakage currents in diodes have a large temperature dependence. They double every eight degrees centigrade [21]. Therefore, the isolation times for a warm start could be substantially shorter than for a cold start. A SPICE simulation of the voltage at node $V_x$ using this circuit at different temperatures is shown in Fig. 18. In this plot, we see the wide variation in the charging times for different temperatures.

**Fixed Current Delayed Start-up:** A problem with any delay-based circuit is that there is a maximum reset time associated with it. If any supply voltage start-up transient is longer than some (predetermined) interval, then initialization will fail, and the isolation time may not be sufficient. It is almost always possible to place a maximum bound on the supply voltage start-up transient. However, for those applications where it is not possible to do so, we propose the circuit shown in Fig. 19. This circuit does not turn on until the supply voltage is above a certain voltage threshold. For the design shown, this is greater than three device thresholds. The value of this voltage can be changed by varying the number of transistors stacked. The charging time is a function of the current mirror ratio $M$, device sizes, number of transistors in the stack, and the magnitude of device threshold voltages. The primary advantage of this circuit is that the starting time depends on the supply voltage, and as such, this circuit can adapt to any supply voltage ramp time. It, however, has the disadvantage that the area overhead is higher. It also has an additional drawback of constant power drain during normal operation. In this circuit, the transistors $Q_2$, $Q_3$, and $Q_4$ are always on, thereby resulting in dc quiescent power consumption.

**Discussion:** SIME's are a self-contained design option. Further, their use incurs a very limited cost. All the designs discussed utilize very few transistors for self-initialization. Any area overhead is confined to the ME itself. ME's constitute only a fraction of the active area at the chip level. This further reduces the area impact of the self-initialization circuitry. The primary area overhead for an on-chip reset is that incurred by routing the reset signal globally. The area occupied by signals, which are globally distributed, is disproportionate to the number of transistors, which are gated by these signals. For example, in the 68040 microprocessor [16], global signals account for 5% of the transistors, while they occupy 22% of the area. Therefore, eliminating a global signal will have significant benefits. In terms of overhead, SIME's compare favorably with on/off-chip reset signals.

Similarly, the performance impact is also minimal. In a SIME, the initialization transistor is completely off, and the isolation transistor permanently during normal operation. Nonidealities are introduced by small parasitic capacitances and a nonzero ON resistance. The net effect of the I/V block is the addition of an inverter in the signal path. This results in a minor increase in the hold time. In general, in synchronous sequential circuits, the clock period is much larger than the hold time of a ME. Hence, in practice, the performance impact may be negligible or nonexistent. In many designs, the strengths of the drive transistors at the input to each SIME in the circuit are predictable. This removes the need for isolation during initialization. By removing the isolation component and appropriately placing the initialization transistor, the performance impact can actually be eliminated.

As mentioned earlier, on-chip reset signals have been suggested previously. An on-chip reset signal generation technique, based conceptually on an $RC$ delay, has been discussed in [4]. However, no circuit level implementations to realize the $RC$ delay are discussed. Naive circuit implementations can make this technique completely impractical. For example, a passive $RC$ implementation of the delay structure, for a microsecond delay, could easily occupy half the chip area.
It is necessary to generate designs that are both viable and practical. Hence, in this paper, as a prelude to discussing our reset generation techniques, we have analyzed the start-up environment in detail. Any one of the designs developed will not occupy any significant chip area. The RC-based design is similar in concept but more specific in detail compared to the technique in [4]. The two other techniques, leakage current-based are new techniques to generate a delayed signal, which have not been discussed previously. Since our designs are so economical, we have suggested that each ME in a circuit actually be provided with its own initialization circuitry. Further, we will demonstrate that SIME's have distinct advantages in circuit test. An individual ME's initialization circuitry may be overpowered by signals from the rest of the logic during start-up. Hence, our approach also requires the development of techniques to isolate an ME during start-up.

The choice of a particular SIME design is circuit specific. As with the active RC-based design, solutions for the isolation times can be calculated for all the topologies. The RC and leakage current-based designs have a lower area overhead compared to the fixed current start-up. However, the start-up circuit cannot handle extremely long risetimes for the power supply voltage. The constraint on the rise time arises from the fact that for extremely long risetimes the current due to weak inversion operation finally charges up node $V_s$ to $V_{DD}$. Thus, even though initialization may occur the necessary isolation cannot be guaranteed. In contrast, the fixed current-based designs result in both a higher overhead and in constant power consumption. Overall, the reverse leakage current circuit is the most compact and would be most appropriate if the variations in the start-up times can be tolerated. This design provides the best cost-benefits trade-off.

IV. APPLYING SIME'S TO CIRCUIT TEST

SIME's may be used in many applications instead of (on- or off-chip) reset signals. We concentrate on the application of SIME's to the problem of test generation for synchronous sequential logic circuits. For analysis, we use the common single stuck-at model [4].

Analysis

First, we consider the effects of faults internal to the SIME's. Without the loss of any generality, we will only consider SIME 0's. Our analysis can be easily extended to SIME 1's. The logic diagram for a SIME 0 is shown in Fig. 20.

The only global lines are the $V_{DD}$, $V_s$, and read/write lines. Techniques developed by others may be used to detect faults in these lines [4]. Our analysis assumes that a block appropriate to the needs of the application has been chosen. Excluding the global lines, all signal lines in Fig. 20 have been assigned unique numbers. Each line has two faults, a stuck-at-zero (sa0) fault and a stuck-at-one (sa1) fault associated with it. For a sa1 fault, we assume the voltage at the site of the fault rises at the same rate as does the power supply. There are a total of 18 single stuck-at faults to be analyzed. We analyze faults on each line individually.

Line 1: Clearly, the fault 1 sa0 will permit correct initialization. However, it will affect normal operation. The fault 1 sa1 will affect the value on line 8 (the output) as long as the switch conducts. We assume that the delay provided by the I/I block is sufficient to allow the signals controlling the switch to settle. This implies that the fault 1 sa1 cannot affect the initial state of the SIME. However, it too corrupts normal operation.

Lines 2, 7, 8, 9: Single sa0 faults on any one of these lines will permit the SIME to initialize to the desired initial state. However, they will affect normal operation. The output is forced to 0 permanently. Single sa1 faults on these lines force an initial value, which is in conflict with the desired value. In a SIME, for any I/I block design, the strength of the signal provided by the I/I block decreases with time. In contrast, a sa1 fault will ramp up with the power supply and remain at constant strength therefor. Hence, a permanent stuck-at fault will dominate the initialization circuitry. Therefore, single sa1 faults on these lines will initialize the SIME to the wrong initial state and affect the operation of the CUT.

Line 3: The fault 3 sa0 is equivalent to the fault 2 sa0. The functional effects of equivalent faults are identical. The fault 3 sa1 may be analyzed as follows: The voltage at a stuck at 1 fault site rises with $V_{DD}$. Hence, this fault is equivalent to a zero or lower than expected isolation time provided by the isolation block. In the worst case, the initializing PMOS transistor is never turned on. Therefore, the initial state of the SIME in the presence of this fault cannot be predicted. However, it does not affect the normal operation of the SIME and the CUT.

Lines 4, 5, 6: The fault 5 sa0 is equivalent to the fault 7 sa1. Similarly, the fault 5 sa1 is equivalent to 7 sa0. The functional effects of equivalent faults are identical.

From the above discussion, it can be seen that the faults in a SIME can be grouped in three broad categories.

Class A: Faults that affect the initial state only.
Class B: Faults that corrupt normal operation and not the initial state.

Class C: Faults that corrupt both normal operation and the initial state.

Table I shows the distribution of faults among the various classes. In the next section, we discuss how existing TPG algorithms are constrained by SIMES’s.

**Test Generation Constraints**

In comparison to a reset signal, SIMES’s place additional constraints on a test generation/fault simulation system. In general, test generation is an iterative process. Given a circuit to be tested, initially a list of all modeled faults is compiled. The first fault on the list is targeted for test generation. If a test sequence is successfully generated, a fault simulator is used to verify if other faults are coincidentally detected by the same sequence. All detected faults are eliminated from the fault list. The generation of test sequences continues until all faults have been detected. In a circuit with a reset signal, the circuit can be reset after the application of each test sequence. Circuits employing SIMES’s cannot be reset after each test sequence. Both the test generation and fault simulation algorithms will have to account for this.

Essentially, with a reset signal, after each sequence, the test generation system can “synchronize” the states of the good circuit and all remaining faulty circuits. This is not possible in a circuit using SIMES’s. As demonstrated in Section 4.1, the initial states of the good circuit and all faulty circuits are known. The vectors in the test sequences and their order of application are also known. Hence, it is possible to track the states of the good and remaining faulty circuits after the application of each test sequence. In other words, though the good circuit and all faulty circuits cannot be reset simultaneously, it is possible to individually identify the state of the good and each faulty circuit after each test sequence. To accomplish this, the fault list data structure will have to be augmented. Faults in the combinational logic block do not affect the initial states of the SIMES’s in a circuit. However, if they are not redundant, they will corrupt transitions in the circuit. Irredundant faults in the combinational logic, class B, and class C SIMES faults all corrupt transitions in the circuit under test. Thus, traditional sequential circuit test generation techniques may be used to detect these faults. However, class A faults do not affect transitions in the CUT. They have to be addressed separately.

**Reset Verification:** Prior to developing techniques to detect class A faults, a preliminary definition of notation will be useful. In a CUT with \( n \) SIMES’s, let the correct reset state be \( R = r_{n-1} \ldots r_1 r_0 \). Denote a class A fault in SIME \( i \), \( 0 \leq i \leq n-1 \), by \( f^{A_i} \). Class A faults may affect the initial state of the CUT. A fault \( f^{A_i} \) can cause the erroneous reset state to be \( R_i = r_{n-1} \ldots r_{i+1} \bar{r}_i r_{i-1} \ldots r_0 \), where \( \bar{r}_i \) denotes the complement of \( r_i \). Denote \( \{ R_i \} \) by \( R_{UD} \). In words, \( R_{UD} \) consists of the set of all states at unit distance from the reset state. An example will serve to illustrate the constraints on the detection of class A faults. Consider the transition table shown in Fig. 21.

This circuit has one input pin and one output pin. Let \( R = 00 \). Consequently, \( R_0 = 01 \) and \( R_1 = 10 \). We will refer to the fault-free circuit by \( M \) and the faulty circuit in the presence of class A faults \( f^{A_0} \) and \( f^{A_1} \) by \( M_0 \) and \( M_1 \), respectively. Assume that the circuit has been powered up and is to be tested for the class A faults. The input sequence (of length 1) \( I = 0 \), distinguishes between \( R \) and \( R_0 \). For this sequence, \( M_0 \) and \( M_0 \) produce outputs of 0 and 1, respectively. Hence, I detects \( f^{A_0} \). However, for an input of \( I = 0 \), both \( M_0 \) and \( M_1 \) will transfer to state 01. Thereafter, the fault \( f^{A_1} \) cannot be detected without resetting the circuit with another power-up.

In contrast, the sequence \( I_1 = 10 \) will detect both faults, \( f^{A_0} \) and \( f^{A_1} \). This sequence distinguishes state \( R \) from both states \( R_0 \) and \( R_1 \).

To detect class A faults, a sequence which distinguishes the reset state \( R \) from \( R_{UD} \) is required. We will refer to this sequence as a reset verification sequence. A distinguishing sequence uniquely identifies the initial state of the circuit. Let \( S \) be the set of all states in the circuit other than the reset state. A UIO [11] sequence for the reset state \( R \) will determine if the initial state of the circuit is \( R \) or is a member of \( S \). Both a distinguishing sequence and a UIO sequence for \( R \) are reset verification sequences. Though a circuit may not possess a distinguishing sequence, it may possess a UIO sequence for the reset state. Further, UIO sequences are known to be easier to generate. Further, \( R_{UD} \subseteq S \). Hence, even when a circuit does not possess a UIO sequence for the reset state, it may possess a reset verification sequence. Reset verification sequences can potentially be generated in one of two ways. If a functional description of the CUT is available, algorithms used to generate UIO sequences [11] can be easily modified to generate reset verification sequences. If the only available description is at the gate level, propagation sequence generation algorithms [4], [9] can also be directly extended to generate reset verification sequences. We believe no advantage is to be gained by further detail. Readers are referred to the relevant publications [4], [9], [11] for more detail.

In summary, SIMES’s require less overhead than do reset signals. However, in comparison to off-chip reset signals, SIMES’s place more constraints on a test generation/fault simulation system.

**TABLE I**

<table>
<thead>
<tr>
<th>Class</th>
<th>Members</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3sa1</td>
</tr>
<tr>
<td>B</td>
<td>1sa0, 1sa1, ( {2,3,6,7,8,9} ) sa0, 5sa1, Comb. Logic</td>
</tr>
<tr>
<td>C</td>
<td>( {2,3,6,7,8,9} ) sa1, 5sa0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Present State Input</th>
<th>Next State, Output Input=0</th>
<th>Input=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01, 1</td>
<td>11, 1</td>
</tr>
<tr>
<td>01</td>
<td>11, 0</td>
<td>00, 0</td>
</tr>
<tr>
<td>10</td>
<td>01, 1</td>
<td>00, 0</td>
</tr>
<tr>
<td>11</td>
<td>10, 0</td>
<td>11, 0</td>
</tr>
</tbody>
</table>
V. CONCLUSION

In this paper, we presented a new type of memory element, a self-initializing memory element. SIME's are designed to individually start up to a predetermined internal state at power-up. The various SIME designs utilize low cost initialization techniques, each of which has been described in detail. The start-up environment in a ME was analyzed in detail. This analysis accounted for the effects of both flicker and thermal noise during the start-up period. The results of this analysis were used to design and validate several different types of SIME's. In this specificity and in providing each ME with its own initialization circuitry, our technique differs from previous general approaches. Each SIME design offers a different benefit-overhead trade-off. The user's requirements will dictate the design choice in a particular application. The area and performance impact of SIME's was shown to be minimal. The application of SIME's to the problem of test generation was also discussed. They provide a designer with an additional option, which offers different area-benefit trade-offs in comparison to other solutions to the initialization problem. The development of a sequential circuit test generator for a circuit-employing SIME's remains to be addressed.

REFERENCES


Bapiraju Vinnakota (S'89–M'91) received the B. Tech. degree from the Indian Institute of Technology, Madras, India in 1987 and the Ph.D. degree from Princeton University, Princeton, NJ in 1991, both in electrical engineering. He is an Assistant Professor with the Department of Electrical Engineering at the University of Minnesota, Minneapolis. He also held a short-term position at AT&T Bell Labs in 1990. His research interests include digital system testing, CAD for testing, analog and mixed-signal circuit testing and fault-tolerant computing.

Ramesh Harjani (S'87–M'89) for a photograph and biography, see p. 376 of the June 1995 issue of this TRANSACTIONS.