A Low-Power CMOS VGA for 50 Mb/s Disk Drive Read Channels

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Abstract—We describe an all CMOS variable gain amplifier (VGA) suitable for use in disk drive read channels. The VGA maintains a 3 dB bandwidth greater than 85 MHz throughout its gain range. This ensures good phase linearity for data transfer rates of up to 50 Mb/s. The VGA provides a 25 dB gain variation along an ideal exponential gain to control voltage curve and 30 dB of gain control if ideal exponential characteristics is not absolutely necessary. The VGA achieves the necessary exponential gain to control voltage characteristics intrinsically using only MOS transistors as a single unit to reduce power and area consumption. Overall power consumption is less than 10 mW for the VGA circuit excluding the off-chip buffer circuits.

I. INTRODUCTION

THE desire for smaller drives with reduced power consumption increases the need to integrate the read channel electronics into a single mixed-signal CMOS chip or a set of chips. Variable gain amplifiers (VGA) form an important component of the read channel and help stabilize the voltage supplied to the detector and filter sections of the read channel. Standard bipolar VGA's [1] dissipate lots of power and previous attempts at developing a CMOS compatible VGA [2] have resulted in variable gain amplifiers with the necessary gain control characteristics but still dissipating substantial power. A significant percentage of this power is dissipated in generating the exponential current output for a linear voltage input. The exponential gain to linear control voltage characteristic is preferred for read channel automatic gain control loops [1]–[4] to minimize variations in the output voltage. Here we present a methodology for generating the desired exponential transfer characteristics intrinsically using only MOS devices within the variable gain amplifier structure. It is usually not possible to operate the MOSFET in the weak inversion region because of the high frequencies involved in the signal path of read channels. Therefore, for these frequencies in CMOS there is no intrinsic logarithmic device transfer characteristics that can be exploited to generate the necessary exponential gain to linear control voltage characteristic desired. One possible methodology to generate this exponential characteristic is to use the parasitic lateral bipolar transistors available in CMOS [2], [5], [6]. An alternate methodology, being presented here, is to use the exponential gain control behavior presented by the function

\[ \text{Gain} = \begin{cases} 
\frac{1+x}{1-x} & 
\text{if } x > 0 \\
\frac{1-x}{1+x} & 
\text{if } x < 0 
\end{cases} \]  

(1)

\[ \text{Gain range} = \frac{(1+x)^2}{(1-x)^2} \]  

(2)

This expression is plotted in Fig. 1, where the y scale is in dB's. It is possible to see that the gain expression in (1) provides the necessary exponential transfer characteristics and shows a good match for \(-0.7 < x < 0.7\). Further, it can be shown that the maximum gain range is given by (2). Therefore, for a gain range of 30 dB the value of \( x \) needs to be varied from -0.698 to +0.698. As just mentioned, the exponential characteristics matches fairly well within this range. Outside this region \((-0.7 < x < 0.7\) the rate of change in gain is even more rapid. As it turns out this provides even better control of the output voltage in comparison to a simple exponential gain characteristics. A comparison of the output voltage produced using the normal exponential scheme and our scheme is shown in Fig. 3. The system level block diagram, shown in Fig. 2, for the automatic gain control loop was used to obtain the voltages in Fig. 3. The value of error voltage amplification, \( K \), was set to 1. A higher value of \( K \) would lead to better output control for both schemes. However, for comparison purposes any value is appropriate. For the two schemes only the transfer function block between \( E_c \) and \( A \) was changed. We note in Fig. 3 that at both higher and lower input voltages our scheme performs better than an ideal exponential in maintaining a constant output voltage. Therefore, the value of \( x \) could be varied beyond \( \pm 0.7 \). However, varying \( x \) beyond these limits has detrimental affects on bandwidth and phase characteristics and is discussed later.

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two source follower stages to drive external loads of 5 pF, as in [2]. During normal operation the VGA will be followed by other on-chip circuitry, usually a detector, and the source follower stages can be dropped. A careful look at the first two stages will show that they are vertically flipped mirror images of each other. For example, transistors $Q_2$ and $Q_3$ provide the same functionality for the second stage as do transistors $Q_5$ and $Q_4$ for the first stage. This allows the circuit topology to be extended from one variable gain stage to $n$ variable gain stages, where the value of $n$ is only limited by power consumption, circuit noise and the total phase contribution. Increasing the number of stages increases the range of gain variability possible. For example, four such stages could be used to provide 60dB of gain variability.

As both the gain control stages operate similarly we will discuss only the first stage. Transistors $Q_3$ and $Q_4$ are diode connected and operate as the load transistors for the differential pair $Q_2$ and $Q_3$. The gain for the first stage is controlled by the ratio of the transconductances of $Q_2$ and $Q_3$ (and $Q_1$ and $Q_3$), $\{\text{gain}_{\text{stages}} = \frac{gm_2}{gm_1}\}$. The ratio of their transconductances can be varied by changing the ratio of the currents that pass through $Q_2$ and $Q_3$. The current flowing through $Q_2$ and $Q_3$ are given by

\[
I_{Q_2} = \left(\frac{2I_b + 2I_1}{2}\right) = I_b + I_1 = I_b \left(1 + \frac{I_1}{I_b}\right)
\]

\[
I_{Q_3} = I_{Q_2} - 2I_1 = \left(\frac{2I_b - 2I_1}{2}\right)
- 2I_1 = I_b - I_1 = I_b \left(1 - \frac{I_1}{I_b}\right)
\]

The gain of the first stage can therefore be altered by changing the value of the current $I_1$ and is equal to

\[
\text{Gain}_{\text{stages}} = \sqrt{\left[\frac{\frac{gm_2}{\frac{W}{L_2}}}{\frac{gm_1}{\frac{W}{L_1}}}\right] \left[\frac{1 + \left(\frac{I_b}{I_b}\right)}{1 - \left(\frac{I_1}{I_b}\right)}\right]}
\]

The left half of the gain expression given by (5) is a function of device sizes and process parameters and is a constant during normal use. The right half has the form $\sqrt{\frac{1 + x}{1 - x}}$. As mentioned earlier, except for the square root this expression has the exact form we desire. To compensate for the square root we use two stages and vary the current $I_1$ from $-0.7I_b$ to $+0.7I_b$ to achieve the necessary 30 dB of gain variation. Currently a simple class-A current amplifier is used to generate the current $I_1$. Alternately, a class-AB current amplifier design [9] can also be used and will further help reduce power consumption. However, care must be taken to reduce crossover distortion or VGA gain hunting is likely to occur.

The voltage sources $(V_{\text{off}})$ are included to allow the current sources of the second and third stages to operate in the saturation region. The value of 0.4 V for this offset voltage is selected such that it is greater than the $(V_{gs} - V_t)$ of the current sources but is small enough such that it does not have much impact on the input common mode range of the VGA.
This offset voltage is generated using a feedback scheme that provides a low impedance voltage source and is shown in Fig. 5. Fig. 6 shows the SPICE simulation results for the offset voltage generator. When the load current approaches 100 nA, the offset voltage rapidly rises to 0.4 V and then remains fairly steady even when the load current increases to 100 µA. If common mode range is not of concern then a simple diode connected transistor can be used instead. Transistor Q32 is operated in the subthreshold region and transistors Q31, Q33 and Q34 are operated in strong inversion. Transistor Q34 is in the triode region and acts as a resistive load for transistor Q32. The low resistance at this node is included to stabilize the loop by increasing the pole frequency formed at the drains of Q32 and Q34. As soon as the gate to source voltage of Q32 is sufficiently large (approximately equal to $V_{off}$) the drain current of Q32 increases and pulls up the gate of transistor Q33. This in turn rapidly increases the gate to source voltage of transistor Q31 and $V_{off}$ does not increase beyond the desired value. The circuit in Fig. 5 functions in manner that is similar to a series voltage regulator except here we fix the voltage drop across the load transistor rather than the output voltage. Since the necessary $\Delta V_{gs}$, ($\Delta V_{gs} = V_{gs} - V_{t}$), is small the turn on voltage for transistor Q33 is approximately equal to $V_{tn}$. Using this constraint, the desired offset voltage, $V_{off}$, can be set using (6).

$$V_{off} = \eta U_T \ln \left[ \frac{K_n L_{32} W_{34}}{I_{d0}} \frac{W_{34}}{L_{34}} (V_{DD} - \frac{3}{2} V_{tn}) V_{tn} \right]$$  (6)

Here $U_T$ is equal to $KT/q$ which is approximately equal to 26mV at room temperature, the slope factor $\eta$ is usually between 1.3 and 2 and is fairly controllable [10], $K_n$ is the transconductance parameter for NMOS transistors, $W_{32}$, $L_{32}$, $W_{34}$ and $L_{34}$ are the widths and lengths of transistor Q32 and Q34. $I_{d0}$ is a process dependent parameter and is highly unpredictable. However, $I_{d0}$ affects the offset voltage only logarithmically such that a 100% variation in $I_{d0}$ only causes a 6% variation in the offset voltage. The other parameters are likely to have much smaller variation. The loop gain for the offset voltage generator with a load capacitance of 5 pF is shown in Fig. 7 and the closed loop source impedance of the generator is shown in Fig. 8. The source impedance of a diode connected, 1 /$gm$, transistor is also shown in Fig. 8. We note that the source impedance for the offset voltage generator is lower than that for the diode connected transistor for low frequencies (36 $\Omega$) and increases at higher frequencies. This results in a slight degradation of the CMRR at these frequencies. However, as mentioned earlier, the dc voltage drop across the diode connected transistor is larger.

An expanded view of the third stage is shown in Fig. 9. Previously, transistors Q11, Q12, Q15, Q16, Q19 and Q20 were omitted from Fig. 4 for clarity. Transistors Q15 and Q16 are identical in size to Q9 and Q10 and are used to cancel the Miller multiplication effect. Transistors Q19 and Q20 are primarily included to reduce the negative feedback effect of the transistors Q15 and Q16 [14]. However, they also function to reduce the gate-to-source capacitive loading effects of transistors Q15 and Q16. The third stage is set to have a large gain as a result of which the drain-to-gate capacitance
effective gate referred capacitance for this circuit is given by
(7), where \( A \) is the gain of the third stage. When transistors \( Q_9 \)
and \( Q_{15} \) are matched this equation can further be simplified to
(8).

\[
C_{eff} = C_{gd9}(1 + A) + C_{gd15}(1 - A) + C_{gs9}
\]

\[
+ C_{gs15}\left(\frac{gds19}{gm_{15} + gds19} \right)
\]

(7)

\[
C_{eff} \approx 2C_{gd9} + \left[ 1 + \left(\frac{gds19}{gm_{15} + gds19} \right) \right] C_{gs9}
\]

(8)

In comparison, the gate referred capacitance for the regular
cascade technique is equal to \( 2C_{gd} + C_{gs} \) and the gate
referred capacitance for a noncascade noncanceled circuit
is equal to \( C_{gs} + (1 + A)C_{gd} \). Unlike normal
 cascading techniques, the addition of the two extra transistors \( Q_{15} \)
and \( Q_{16} \) increases the gate-to-source capacitances slightly.
However, the effect of this is much smaller than the effect
caused by Miller multiplication because of the large gain
associated with the third stage. For example, for our circuit
for a value of \( 1/gds_{19} = 50K \) the effective gate referred
capacitance is only 12% larger than for a regular cascade. As
shown in (7) it is important that the two capacitances \( C_{gd9} \)
and \( C_{gd15} \) match fairly well for complete cancellation.
The gate to drain capacitance is a function of the lateral diffusion
of the drain junction and is highly process dependent. Therefore,
it is important that identical methods be used to generate both
capacitances. We use identical device sizes for this purpose.
The drain-to-gate capacitances of transistors \( Q_{15} \) and \( Q_{16} \) are
used to cancel the effects of the drain-to-gate capacitances of
\( Q_9 \) and \( Q_{10} \).

Unfortunately, transistors \( Q_{15} \) and \( Q_{16} \) also provide nega-
tive feedback which reduces the gain of the third stage. For
this reason values for \( gds_{19} \) and \( gds_{20} \) are selected such that
the transconductances of transistors \( Q_{15} \) and \( Q_{16} \) are much
smaller than those of \( Q_9 \) and \( Q_{10} \). Therefore, the gain is only
reduced slightly. The resulting effective transconductance is
given by (9). Since the sizes of \( Q_9, Q_{10} \) and \( Q_{15}, Q_{16} \) are
the same their transconductance is set by the current flowing
through them. The relationship between the currents trough
\( Q_9 \) and \( Q_{16} \) are given by (10). For our design the reduction

\[
(C_{ds}) \text{ of } Q_9 \text{ and } Q_{10} \text{ get Miller multiplied and lowers the bandwidth of the second stage. Traditionally, cascading [5] is used to reduce the Miller multiplication effect. Unfortunately, cascading also limits the maximum swing possible from the amplifier. For this reason we use the partial positive feedback scheme to reduce Miller multiplication effects. A simplified schematic to calculate the effective gate referred capacitance of the third stage is shown in Fig. 10. It can be shown that the}

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\]
in the transconductance is approximately four percent. At extremely high frequencies the gain of the third stage becomes sufficiently small due to its own bandwidth limitations and the Miller multiplication effect becomes insignificant. In Fig. 12 we plot the gain versus frequency for the second stage with and without our Miller cancellation circuit. The heavy line shows the result after Miller effect cancellation and the thin line shows the result without any cancellation. In this figure we note the reduction in gain due to Miller multiplication and also the reduction of this multiplication effect at higher frequencies. We also note that the plot is smoother after cancellation, i.e. more constant group delay. The Miller multiplication effect has been canceled but there is a slight reduction in the overall bandwidth due to the increase in the gate-to-source capacitance. The transistors $Q_{12}$ and $Q_{16}$ primarily affect the high frequency ac behavior and so the overall circuit can effectively be simplified by removing $Q_{15}, Q_{16}, Q_{19}$ and $Q_{20}$ and assuming that the gate-to-drain capacitances of transistors $Q_9$ and $Q_{10}$ are zero and that the effective transconductance of $Q_{15}$ and $Q_{16}$ are reduced slightly,

$$gm_{eff} = gm_0 \left[ 1 - \frac{gds_{20}gm_{16}}{gm_0(gm_{16} + gds_{20})} \right]$$  \hspace{1cm} (9)

$$Ids_{15} = \frac{\sqrt{2K_n^*W_{15}I_{ds_0}gds_{20}}}{gds_{20}} + \sqrt{1 + \left( \frac{\sqrt{2K_n^*W_{15}}I_{ds_0}gds_{20}}{gds_{20}} \right)^2 K_n^*W_{15}gds_{20}}$$ \hspace{1cm} (10)

The output stage is designed to provide a large bandwidth and large dynamic range at low distortion. This is achieved by using transistors $Q_{11}$ and $Q_{12}$ in the triode region. Two transistors are used instead of one to cancel higher order signal distortion due to variations in threshold voltage as a result of changes in the source to bulk voltage, $(V_{sb})$ of the load transistors. The circuit topology also allows for some independent control of the differential mode and common mode gain and bandwidths. The midpoint between the two transistors is fairly constant for differential mode signals. Therefore, $C_m$ has no effect. However, for common mode signals $C_m$ acts as an additional load. Transistors $Q_{13}$ and $Q_{14}$ provide common mode feedback and control the dc voltage at the outputs of the third stage. This topology for common mode feedback [11], [12] is particularly attractive for high frequency applications and provides a number of advantages when compared to other topologies [12], [13]. First, the circuit does not add any additional high impedance nodes in the circuit that can add phase and affect the stability of the common mode feedback loop. Second, the two transistors $Q_{13}$ and $Q_{14}$ operate in the triode region and provide a low impedance node at the source nodes of transistors $Q_{17}$ and $Q_{18}$. The differential mode gain for this stage is set by the triode operated transistors $Q_{11}$ and $Q_{12}$ and is given by $(11)$. As mentioned earlier for differential mode signals $C_m$ has no effect. Additionally, for differential mode signals the common mode feedback circuit has no small-signal effect and the impedance looking into the drains of $Q_{17}$ and $Q_{18}$ are high. Therefore, the primary resistive load at the outputs is approximately equal to the inverse of the conductance of $Q_{11}$ and $Q_{12}$. Therefore, the bottom half of the circuit can be replaced with a simple differential pair with zero gate to drain capacitance and slightly lower transconductance.

$$\text{Gain}_{DM_{\text{stage}3}} = \frac{-gm_0 gds_{11}}{gds_{11} + \frac{1}{\text{gm}_{22}} (1 + \frac{\text{gm}_{22}}{gds_{11}})}$$ \hspace{1cm} (11)

The common mode gain for a completely balanced circuit is ideally zero. However, any imbalance between the two sides results in some nonzero common mode gain. This is illustrated in Fig. 18. For this simulation the threshold voltage of transistor $Q_9$ was altered by $10mV$. We note both a nonzero common mode gain and also the beneficial effect of adding $C_m$. Though a complete analysis for common mode gain is not provided as this would entail listing the influence of each transistor in the third stage and all of their parameters. However, a qualitative explanation can be provided for the $V_t$ offset situation just mentioned. Other situations can be analyzed similarly. The common mode gain for each half of the circuit is given by the ratio of the conductances $g_0/g_l$. Here $g_0$ is the conductance of the current source $I_L$ and $g_l$ is the effective conductance looking into the drain of transistor $Q_{17}$ with the common mode feedback circuit being functional. The low frequency value of $g_l$ is given by $(g_{m12}g_{m13})/(g_{ds13} + g_{m17})$. The offset voltage is amplified by the gain of the third stage and causes the two output voltages to be different. This in turn causes the effective $g_l$ of the two halves to be different. The transconductance of $Q_{17}$, $(g_{m17})$, essentially remains the same because of the extremely small change in the current due to this change in the output voltage. Likewise, the transconductance of $Q_{13}$, $g_{m13} = [(k_p^*W/L)V_{ds13}]$, also essentially remains the same as the $V_{ds}$ is maintained constant by the common mode feedback effect. However, the conductance of $Q_{13}$, $gds_{13} = (k_p^*W/L)(|V_{gs13} - |V_{tp} - |V_{ds13}|)$, changes because $V_{gs13}$ changes due to the difference in the two output voltages. This causes the conductance looking into the drain of $Q_{17}$ to be different for that looking into the drain of $Q_{18}$. Therefore, the gains of the two halves are not equal and this results in the nonzero common mode gain.

Due to the fully differential structure of the VGA any common mode signal at the input of the first stage is severely
attenuated by the first two stages before it gets to the output stage, i.e., the overall VGA has a fairly high common mode rejection ratio (CMRR). Therefore, one of the primary purposes of the common mode feedback circuit in the output stage is to stabilize the output voltage in the face of process and temperature variations. The primary source of such variations are possible changes in the threshold voltages of the transistors, particularly those of $Q_9$ and $Q_{13}$. It also serves to reject any other common mode signals that may arrive at the third stage via the supplies or the substrate. Additionally, because of the complete symmetry maintained throughout the design the power supply rejection ratio is extremely high for this circuit.

The gain of the VGA is controlled by varying the current $I_1$. However, these variations in the current $I_1$ affect the transconductances of the differential pairs and diode connected loads as well. This change in the load transconductances also affects the bandwidth of the first two stages. To reduce the effects of this change in bandwidth on the overall group delay the bandwidths of the three stages are selected so that the bandwidth of the first two stages is much larger than the bandwidth of the third stage. Therefore, the bandwidth of the overall amplifier is dominated by that of the third stage, which is kept constant. One of our design goals is to maintain a fairly constant group delay through the system. In general, the variation in the group delay is minimized by maintaining the poles close to the real axis. For a three stage system like ours the delay through the system is given by (12). Here, $\omega$ is the frequency in radians and $w_1$, $w_2$ and $w_3$ are the three system poles. The variation in the group delay with frequency cannot be made to be equal to zero for such a system. However, it can be minimized within a frequency band by setting the values of $w_2$ and $w_3$ to be approximately equal to 2.23 times $w_1$. This value was generated by setting $w_2 = w_3$ and finding the minimum of the derivative of (12). In our system, the third stage pole is selected to have the lowest frequency as this pole frequency does not change with gain settings. The poles of the other two stages are selected to be close to 2.23 times the third stage pole.

$$
\text{Group delay} = \frac{1}{w_1[1 + (\frac{w}{w_1})^2]} + \frac{1}{w_2[1 + (\frac{w}{w_2})^2]} + \frac{1}{w_3[1 + (\frac{w}{w_3})^2]}
$$

(12)

We shall see the effects of these and other design choices in the results presented in the next section.

III. RESULTS AND CONCLUSION

The results presented in this section were generated with the help of HSPICE simulations. Simulations were done using both BSIM and level 2 models. The results presented here are primarily those from BSIM models. However, BSIM models tend to be pessimistic about output conductance so results were also confirmed using level 2 models. Unfortunately, level 2 simulations have the limitation that the transconductance is discontinuous with respect to current. Layout parasitic estimates were also included in these simulations. These parasitic estimates were generated by completing a layout for a slightly earlier pass design using the Magic layout editor. The current circuit has been designed for the generic MOSIS 2 micron process.

Three dB bandwidths greater than 85 MHz was achieved throughout the gain range. Fig. 13 shows the gain in dB versus the control voltage and Fig. 14 shows the group delay at 50 MHz versus the control voltage for the variable gain amplifier. From Fig. 13 we find that we were able to generate the desired exponential gain versus control voltage relation. Though we do achieve the 30 dB of variation we see some deviations from the ideal exponential characteristics. We are able to obtain approximately 25 dB variation of gain along the ideal exponential relationship. However, as mentioned earlier, this is an advantage rather than a disadvantage. The slight reduction in the overall gain range (from ideal exponential gain to control voltage characteristics) as compared to the expression described in (1) is due to channel modulation and other short channel effects not included in (1). These effects reduce the effective transconductance for the transistors that control the gain in the first two stages. It is expected that these minor variations from the ideal behavior, as long as they are not abrupt, is unlikely to cause any major problems for the automatic gain control loop. In Fig. 14 we find that the group delay is relatively constant with control voltage changes. In Fig. 15 we show a 3 dB bandwidth of 109 MHz for a control voltage of 0.7 V. Fig. 16 shows the phase versus frequency for the amplifier. To maintain a constant group delay through the amplifier it is necessary that the phase increase linearly with frequency. In Fig. 16, we see that the phase increases linearly with frequency till about 200 MHz which clearly suffices for our operating bandwidth. Fig. 17 shows the harmonic content at the output of the amplifier for a $1.2V_{p-p}$ output signal at 50 MHz. The first two stages use diode connected loads which have large quadratic nonlinearities. Additionally, each of the differential pairs generate quadratic nonlinearities. However, we note that the even harmonics are completely suppressed as might be expected in a fully differential design. The total harmonic distortion for the overall amplifier was less than 0.7% for a $1.2V_{p-p}$ output signal.

One of the primary advantages of generating the exponential gain characteristic intrinsically, rather than use a lateral bipolar, is the reduction in power consumption. For example, the total power consumption for our VGA without the source follower stages is approximately 10 mW. This is approximately a order of magnitude lower than the power.
larger in comparison to an all bipolar implementation [1]. The current design has been designed to operate at 50 MHz. However, it is expected that the basic design can be extended to higher frequencies by going to smaller geometries and/or by increasing the power. Additionally, a larger range in gain variability can be accommodated by increasing the number of stages.

We have described a low-power CMOS variable gain amplifier that uses only MOS devices to generate an exponential gain versus control voltage characteristic necessary for read channel electronics. This paper introduces a number of novel techniques that are used to generate the exponential gain behavior, increase bandwidth, provide a voltage drop less than the threshold voltage and stabilize the group delay.

REFERENCES


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