A 200MHZ DIFFERENTIAL SAMPLED DATA FIR FILTER FOR DISK DRIVE EQUALIZATION.

Ray Barnett  
VTC Inc.  
2800 East Old Shakopee Road Bloomington, MN 55425-1350  
Email: barnett@vtc.com

Ramesh Harjani  
Department of Electrical Engineering  
University of Minnesota  
Minneapolis, MN 55455

ABSTRACT

We describe a 200MHz sample rate analog finite impulse response (FIR) filter suitable for readback equalization in a disk drive channel. The BiCMOS FIR has seven taps all programmable to six bit weights and is implemented in fully differential form. Eight bit linearity is maintained in each circuit block so that the total FIR linearity is well above the six bits required for disk drive electronics. The FIR uses a new track and hold architecture which reduces power consumption over previous architectures while providing high speed operation. Total power consumed is 150mW for a 5 volt supply.

1. INTRODUCTION

Along with the emerging techniques of partial response maximum likelihood (PRML) and fixed delay tree search (FDTSS) into disk drive data detection electronics comes the need for signal equalization prior to the detector [1]. The equalization is often performed using a sampled data FIR filter. In a disk drive read channel there are both digital and analog high speed circuits operating on a single chip. This leads to the use of bipolar high speed current mode logic (CML) digital circuits and fully differential analog signal processing as opposed to CMOS circuits which tend to be more noisy than CML and can corrupt the critical analog circuitry [2]. Thus bipolar techniques also carry over into the FIR filter because of the need of a high speed sampling clock which is best designed in CML to minimize the clock noise generated.

The FIR is based on a circular delay line architecture [3]. This architecture is well suited for an analog implementation since the TH circuits are operated in parallel instead of the traditional series tapped delay line such that offsets and noise are not accumulated in each subsequent stage. Furthermore this architecture is expandable to more tap weights without added circuitry in the direct signal path so that offsets and noise do not build as taps are added.

2. FIR ARCHITECTURE

The seven tap FIR architecture is shown in Figure 1 and its transfer function is given by:

\[ H(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + a_5 z^{-5} + a_6 z^{-6} \]  (1)

If \( n \) equals the number of taps the architecture requires \( n+1 \) track and hold circuits, \( n \) multiplying DACs for the tap weights and \( n+1 \) multiplexers to circulate the signal through the multipliers. For a seven tap FIR; 8 TH’s, 7 multiplying DACs and 8 analog multiplexers are required. In addition an analog summer is needed to perform the summation of the delayed and weighted signals. The circular delay line has the disadvantage of requiring a clocking controller to circulate the samples to the tap weights as opposed to a tapped delay line which only requires a simple clock. This clocking controller consumes about half the total power of the entire FIR. The clocking controller’s function is to generate track/hold and multiplexing signals needed to implement the circular delay line architecture. This architecture is now described.
First one of the 8 TH's tracks the signal for one clock cycle. For the following seven clock cycles the TH is in hold mode and is storing the value sampled at the end of the track cycle. During the first clock cycle in hold mode the sampled value is multiplexed to the a0 multiplier corresponding to the first coefficient in the delay line equation (see equation 1). On the second clock cycle in hold mode the stored value is multiplexed to the second multiplier which is a1 in equation 1. The multiplexing process continues on each clock cycle thus cycling through all the tap weight multipliers. This process simulates a tapped delay line without passing the sampled value into series TH cells on each clock cycle. This has the advantage of not propagating offsets and noise from one TH to the next. The output of the multipliers is summed on each clock cycle the same as the traditional tapped delay line. The resulting output has the transfer function given by equation 1. It is easily seen that only one of the 8 TH's are in track mode at a time and the remaining are all in hold mode. This makes it desirable to reduce the power consumed in the hold mode for each TH so that the total power of the FIR is minimized. The new TH proposed is well suited for the circular delay line architecture since it reduces the power consumption needed during hold mode as opposed to previous high speed bipolar TH's which consume the same amount of power in the hold mode as they do in track mode [4].

3. TRACK AND HOLD ARCHITECTURE

The TH architecture takes advantage of the circular delay line architecture since only one of the 8 TH’s are in track mode at any one time. The new architecture is shown in Figure 2. This architecture uses fast vertical PNP's which are common in processes that are used for disk drive read channels.

The new TH consists of a high speed front end transconductance stage that is shared by all stages. This is shown as $Q_{GM1}$, $Q_{GM2}$ and $R_{GM}$ and associated current sources $I_1$, $I_2$, $I_3$ and $I_4$, $I_3$ and $I_4$ are twice that of $I_1$ and $I_2$ so that a bias current equal to that of $I_1$ flows through $Q_1$ and $Q_2$ of the TH that is selected in track mode. The individual TH stage is a folded cascode PNP unity gain amplifier that has NPN emitter followers to drive the hold capacitors. When the TH is in the track mode the PNP cascode $Q_1$ and $Q_2$ is turned on and the bias and signal current are summed and flow through diode connected NPN $D_1$. This in turn mirrors the common mode current into $Q_3$ and $Q_4$ which are the current sources for the emitter followers $Q_3$ and $Q_4$ respectively. The differential current signal between $Q_1$ and $Q_2$ is converted to a differential voltage via resistors $R_1$ and $R_2$. This voltage is then buffered by the emitter followers $Q_3$ and $Q_4$ and the resulting differential voltage is place on the capacitors $C_1$ and $C_2$. In hold mode the transistors $Q_3$ and $Q_4$ are shut off, i.e. the next TH's $Q_1$ and $Q_2$ are turned on. The gain resistors $R_1$ and $R_2$ pull down the bases of $Q_1$ and $Q_2$ without using any current unlike previous high speed all NPN TH architectures [4]. $R_3$ turns off the diode $D_1$ and thus the current mirror ($Q_3$ and $Q_4$) for the emitter followers driving the hold capacitors. This completes the hold action for this cell. The new TH architecture results in an 87% power savings in the TH circuitry over previous TH designs when used in a 7 tap circular delay line FIR. This is accomplished because the hold mode power is reduced from the track mode power in the new TH while in the previous high speed TH's the track and hold mode power is the same. Figure 3 shows the settling time results for the TH circuit. Settling time to 0.4% of the final value for a 500mV p-p differential step input is 3ns. This allows 2ns for the waveform to settle in the subsequent multiplier and summer circuits for 200MHz operation. Following the TH circuit the voltage that is sampled is buffered by a low input current V-I converter that minimizes droop on the hold capacitors. The current signal is then multiplexed to the appropriate tap weight implemented as a multiplying DAC. The signal is then circulated through all the DACs until the next track action takes place on that TH cell.

4. MULTIPLEXING, MULTIPLYING AND SUMMING FOR THE FIR

The multiplexing of the sampled analog signal to the appropriate multiplier is accomplished in the current domain by a fast switching NPN multiplexer. As stated earlier, when the signal is held the output current is multiplexed to the first multiplier corresponding to $a_0$ in equation 1. On the next clock, 5ns later for 200MHz sampling, the signal is routed to the multiplier corresponding to $a_1$. On the next sample time the signal is routed to $a_2$ and so on through the last multiplier. Then the TH which has been in hold mode while the multiplier values are cycled through now goes into track mode. During the output is routed to the supply and does not go to a multiplier. Only the TH’s in hold mode are routed to the appropriate multiplier. This simulates the effect of a tapped delay line where each sample is propagated through a series of TH’s and each of the TH outputs are multiplied by a tap weight corresponding to the samples position in the delay line. The digital controller must select the appropriate TH in track mode and must multiplex the sampled outputs to the appropriate multiplier.
to simulate the tapped delay line.

The multiplication is also done in the current domain with a Gilbert multiplier and the coefficients are programmed using 5 bit plus sign multiplication values. The output of all the multipliers are summed in current mode and converted to voltage using a high band width common base stage. The output is then buffered and driven with emitter followers to the subsequent detection circuitry in the read channel. The linear range for the input and output is 0.5V p-p differential.

5. CONCLUSION

In this paper an analog FIR filter has been presented which operates at 200MHz sample rate and has resolution to 6 bits. The FIR is suitable to be used in a disk drive read channel for signal conditioning. The FIR architecture incorporates a new track and hold circuit which minimizes the power consumption while maintaining high speed acquisition of the signal. The power savings in the TH circuitry for a seven tap FIR is 87% over previous TH designs. This is accomplished by reducing the power in hold mode in the new TH.

REFERENCES


![Figure 1. FIR circular Delay Line Architecture](image)
Figure 2. TH Architecture

Figure 3. Eight bit (0.4%) settling time for TH with 500mV p-p differential input step is 3ns