ANALOG IMPLEMENTATION OF THE FDTS/DF DETECTION ALGORITHM FOR MAGNETIC RECORDING

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Abstract — An analog implementation of the fixed delay tree search algorithm for magnetic recording detection is presented. The circuit is designed using a 1.2um BiCMOS process with NPN devices with an f<sub>c</sub> of 12GHz, and provides a reference for the feasibility of an analog implementation. Composite simulation results of all the system blocks suggest operating speeds in excess of 100MSamples/s with a total power consumption of less than 1W.

I. INTRODUCTION

As computing requirements continue to grow, so do the requirements for larger and faster data storage systems. Magnetic disk drives have dominated the storage market due to their low cost and large storage density. The maximum density of magnetic recording systems is a function of the magnetic media and data retrieval algorithm. Peak detection systems provide a simple means of recovering data [1], but the use of a sequence detection technique such as the fixed delay tree search with decision feedback (FDTS/DF) [2] provides for higher recording density. From fundamental principles it is possible to show that an analog implementation of the FDTS algorithm using 6 bits of accuracy, such as the one presented here, provides greater performance for lower power than a digital implementation [3].

II. FIXED DELAY TREE SEARCH SYSTEM

Fig. 1 shows the detection portion of a read channel of a magnetic recording system. In this figure, the detection process is accomplished by using the basic FDTS/DF algorithm which is shown in the shaded block. The goal of the discrete time analog implementation presented in this paper is to reduce the total power consumption by replacing the computationally intensive digital calculations directly with analog circuits [4]. In addition to the higher power consumption in computations, a digital implementation also requires an additional high speed, high power A/D converter to convert the analog signals from the read head. In contrast, an analog implementation only requires sample and hold circuits, which consume less power.

III. FDTS/DF ALGORITHM IMPLEMENTATION

FDTS sequence detection theory has been presented by Moon, et al.[2]. In its simplest form, the fixed delay tree search is a maximum likelihood detector. The knowledge of the past output sequence and the present sample is used to select the most likely input. The FDTS implementation presented herein has a tree depth of four (1+4), where \( \tau_{\text{delay}} = 3 \). For illustration purposes, a simplified analog implementation of the FDTS with a tree depth of two is shown in Fig. 2. The decision feedback equalizer, not shown, generates an output current which is a function of the previous output data sequence. The operation follows directly from the algorithm [2]. For the simplified schematic, the input sample \( r_{\text{in}} \) is replicated four times. The branch metric coefficients, \( y_i \), where \( 1 \leq i \leq 2^{1+4} \), are subtracted from each sample, and the result is squared and made negative. Each of these new branch metrics, \( \lambda_{1+4} \), is summed with the current parent metric, \( m_1 \), and the average of the previously calculated metrics is subtracted. The subtraction provides a common mode feedback which does not let the analog circuits saturate. These new branch metrics are then sampled and held for use in subsequent operations, i.e. used as parent metrics. The branch metrics are also fed to the maximum detection circuit, which determines which branch metric has the largest value. Selection of top or bottom branch metrics as parents occurs via the multiplexers, which are controlled by the result of the maximum circuit. The overall circuit implementation has been designed for eight bits of accuracy in the FDTS system and for six bits of accuracy in the decision feedback equalizer.

IV. CIRCUIT DESIGN

A 1.2um BiCMOS process with NPN devices with an \( f_c \) of 12GHz was chosen for this implementation. BiCMOS offers significant advantages because digital area and power are
The differential output current of the forward equalizer, discussed in [6], is summed with the differential output current of the decision feedback equalizer and converted to a differential voltage. This signal is buffered by BUF2, which drives the sixteen coefficient processor blocks. For clarity, only one of sixteen branches of the FDTS is shown here. The coefficient processor performs the task of generating sixteen new branch metrics each cycle, i.e., \( r(y)^3 \), where \( r \) is the voltage output from BUF2 and \( y \) is the branch metric coefficient. The core operations of the FDTS are performed by the metric processor. These include summing and replicating branch metrics and parent metrics, storing appropriate parent metrics, averaging branch metrics for the common mode feedback circuit, and determining if the maximum branch metric originates from the top or bottom branches. BUF5 converts the ECL output of the metric processor to a CMOS output.

The FDTS circuit design is shown in greater detail in Fig. 4, and Fig. 5.

The voltage buffers consist of a commonly used high-speed open loop complementary bipolar amplifier [7]. Because of their low output impedance, they are well suited to driving the large load of the sixteen coefficient processors.

The squaring circuit converts the differential input voltage to two differential output currents using degenerated differential pairs. The metric coefficient current is subtracted from each of these, and the two resultant currents are multiplied using a “Gilbert Multiplier” circuit [8]. This four quadrant bipolar multiplier topology was chosen due to its speed and accuracy. Sixteen six bit D/A converters provide the metric coefficients for each branch metric of the coefficient processor. These DAC’s allow for adaptive system architectures or may simply be initialized during diskdrive manufacture.

The feedback summing junction, Fig. 4, provides a low-impedance node via the common base transistor configuration.
at which to sum the output of the squaring circuit, parent metrics and metric average. The output current is converted back to a differential voltage and appropriately level shifted before being applied to the sample and hold and maximum circuits.

The maximum circuit compares each of the sixteen branch metrics and determines if the maximum comes from the top or bottom branches. Determination of the maximum value could be a difficult task if taken literally as an exhaustive comparison must be made. Instead, maximum detection is based upon the premise that if the exponentials of the metrics are summed, the largest of each will be accentuated by the exponential function [2]. e.g. $e^1 + e^3 + e^5 = 2.7 + 7.4 + 148.4 = 158.5$. Clearly the result is dominated by the largest exponential term, $e^5$. Each differential output is first converted to a single ended output voltage. The outputs of the top branches are then exponentiated, summed and compared to the summation of the exponentiated bottom branches. The exponentiation takes the form of a current by using the common emitter transistor pair configuration proposed by Bracken [9]. The output is latched and represents the most likely data input. This signal provides control to the system in the selection of parent metrics as discussed previously.

The sixteen branch metrics are also sample and held for use as parent metrics in subsequent operations using a cascade of high speed bipolar differential track and holds [10]. The cascade is necessary because the held signal must remain valid through the entirety of the next phase. The output of the sample and hold is buffered to provide adequate drive capability in the subsequent stages.

The sample and hold output buffer drives the parent metric feeders and averaging circuits, Fig. 5. This differential output signal is replicated twice as a differential branch parent and applied to the appropriate metric selector. The outputs of the top branch parent metrics and bottom branch parent metrics are multiplexed at the start of a new cycle based upon the outcome of the maximum detector. i.e., either the top or bottom parents will feed the next calculation phase. These parent metrics are subtracted from the current metric calculation at the feedback summing junction.

The averaging circuit converts the differential output voltage of each branch metric into a differential current output. These currents are summed at a low-impedance common-base node to provide a quick settling time. This output is then converted back to a differential voltage which drives sixteen V/I converters. The averaging function is generated by appropriate selection of resistors R3, R4, and R5. This current is subtracted from each newly generated branch metric at the feedback summing junction providing a common mode feedback.

V. SYSTEM RESULTS

The circuit was simulated using HSPICE with BSIM2 models. Simulation results are shown in Fig. 6. The settling times and the timing dependencies for each of the major system blocks are shown in this figure. The power consumption of each block is shown to the right. The overall settling time for the FDTS/DF system with a tree depth of four is 8.5ns, yielding operating speeds in excess of 115MS/s. As shown in Fig. 6, the majority of the power is consumed by the sample and hold circuits. The total power consumption, including buffers and biasing circuitry, for a 5 volt supply is 950mW.

![Fig. 6. Circuit Simulation Results](image)

REFERENCES