Nonlinear Settling Behavior in Oversampled Converters

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Abstract: We present a new analytical model for opamp induced nonlinearity in oversampled converters. This model incorporates both finite slew rate and finite gain bandwidth effects and is valid for both first order and higher order modulators. Theoretical predictions agree very well with measurement results from fabricated ICs. The model consists only of circuit design parameters, and can be utilized to explore design tradeoffs and optimize converter performance. For our design the use of our model resulted in a 40% reduction in power consumption without loss of performance.

1 Introduction

Delta-sigma A/D converters have become increasingly popular for high resolution data acquisition and signal conversion applications. The opamp remains as the most critical component that limits the performance of such converters. Nonidealities in the opamp such as finite gain, infinite slew rate and finite bandwidth result in nonlinearity error in the modulator.

The effect of finite gain and bandwidth in general switched capacitor circuits and ΔΣ modulators have been studied by several authors. In [1], a thorough transient analysis including finite bandwidth and finite slew rate in switched capacitor filters was carried out by assuming linear feedback. However, their results cannot be directly applied here due to the highly nonlinear feedback inherent in the ΔΣ modulators. In [2, 3], computer simulations and Z-domain analysis have been carried out to investigate the effect of finite bandwidth on the modulator performance assuming linear settling. However, because of the large feedback reference voltage used in ΔΣ modulators the opamps are forced to slew during the initial charge transfer transient. This slewing results in nonlinear settling. In [5], the slew rate limitation was incorporated in their opamp settling response and the effect on SNR ratio was studied via computer simulations. In [4], table-based simulations were used to study nonlinear settling. However, none of the above approaches provide analytical models for opamp induced nonlinearity. In [6], the influence of opamp dynamics (slew rate and gain-bandwidth) and nonlinear DC gain on the behavior of a modulator has been analyzed and modeled. Unfortunately, their models were obtained by using power expansion and nonlinear curve fitting. The model provides little or no insight on how performance degradation can be related to circuit and system parameters. Traditionally, in order to avoid slewing distortion, large supply currents have been used resulting in increased power consumption.

It is clear that understanding the nonlinear settling behavior is critical to designing high performance ΔΣ converters. In this paper we develop an analytical framework to understand the nonlinear behavior in modulators. In Section 2, we develop a general nonlinearity error model for a first order ΔΣ modulator. In section 3, we apply the model to the nonlinear settling behavior in ΔΣ modulator. In Section 4, we describe experimental results including measurements from fabricated ICs. In Section 5 we provide some conclusions.

2 Framework development

A simplified circuit diagram for a first order ΔΣ modulator is shown in Figure 1. A non-overlapping two phase clocking scheme is assumed. Let us denote \( Q^+ \) as the total charge transferred from the input capacitor \( C_1 \) and the reference capacitor \( C_2 \), to the integrating capacitor \( C_l \) during the sampling period when the digital output from the comparator is “1”. Likewise, let \( Q^- \) be the total charge transferred when the digital output is “0”. Let \( P \) denote the probability that the digital output is equal to “1”. In another words,

\[
P = \frac{N^+}{N} = \frac{N^+}{N^+ + N^-}
\]

where \( N^+ \) is the number of “1”s output, \( N^- \) is the number of “0”s output, and \( N \) is the number of clock periods for each conversion. The total charge transferred from the input and the reference capacitors to the integrating capacitor within the \( N \) clock periods can be written as

\[
Q(N) = N^+Q^+ + N^-Q^-
\]

or in an alternative form

\[
\frac{Q(N)}{N} = P Q^+ + (1 - P) Q^-
\]
and therefore

\[ P = \frac{Q^-}{Q^- - Q^+} + \frac{Q(N)}{N} \frac{1}{Q^- - Q^+} \]  

The second term on the right hand side of the above equation is nothing but the quantization error and can be made to be arbitrarily small by increasing \( N \). We shall therefore ignore it as we are primarily interested in the nonlinear settling error. The above equation can therefore be reduced to

\[ P = \frac{Q^-}{Q^- - Q^+} \]  

Phenomenologically, we can always express \( Q^- \) and \( Q^+ \) in the following fashion

\[ Q^+ = (C_1x - C_2V_r)K^+ \]
\[ Q^- = (C_1x + C_2V_r)K^- \]  

where \( x \) is equal to \( V_t \). The parameters, \( K^+ \) and \( K^- \), describe any deviation from ideal transfer. This deviation could be a result of nonlinear settling, capacitor nonlinearity or power supply disturbance, etc. For a perfect modulator, \( K^+ = K^- = 1 \). The mean or DC value of the digital output, \( D(x) \), is equal to \( 2P - 1 \). With the help of Equations 5 and 6, we can write

\[ D(x) = \frac{C_1x(K^+ + K^-) + C_2V_r(K^- - K^+)}{C_2V_r(K^+ + K^-) - C_1x(K^+ - K^-)} \]  

The mean value reduces to \( \bar{D}(x) = C_1x/C_2V_r \) when the charge transfer is ideal. The error \( E(x) \) due to the nonlinearity is equal to \( \bar{D}(x) - D(x) \), i.e.,

\[ E(x) = \frac{(K^+ - K^-)(1 - \hat{x}^2)}{(K^+ + K^-) - \hat{x}(K^+ - K^-)} \]  

where \( \hat{x} = C_1x/C_2V_r \) is the normalized input value. It is clear that it is the difference between the two coefficients \( (K^+ + K^-) \) that causes the nonlinear error. The specific expressions for \( K^+ \) and \( K^- \) will depend on the specific mechanism that causes the nonlinearity. The above equation serves as the framework for further investigation.

3 Nonlinear settling error

In this section we apply the framework established in the previous section to the nonlinear settling problem in \( \Delta \Sigma \) modulators. We develop an analytical model to relate the nonlinearity characteristics with circuit parameters.

3.1 Determination of \( K^+ \) and \( K^- \)

The expressions for \( K^+ \) and \( K^- \) can be obtained by understanding the dynamics of the integrator shown in Figure 1. The dynamics of the settling behavior of the integrator depends on the relative magnitude of the initial voltage jump at the negative input of the opamp, \( V_{m_i} \), and the threshold voltage of the differential input transistors, \( \Delta V_{th} \). If \( V_{m_i} \) is larger than \( \Delta V_{th} \), the opamp has to go through a slewing period followed by a settling period. If \( V_{m_i} \) is smaller than \( \Delta V_{th} \), the opamp will only experience pure settling. The change in the integrator output voltage, \( \Delta V_o \), at the end of the integrating period, \( T \), can be expressed as shown in Equation 9.

\[ \Delta V_o(T) = \begin{cases} \frac{Q}{C_1} - \tilde{C} \frac{Q}{C_2} \text{sgn}(Q)e^{-\omega T} & \text{if } T < T_{slew} \\ \frac{Q}{C_1} - \tilde{C} \Delta V_{th} \text{sgn}(Q)e^{-\omega(T - T_{slew})} & \text{if } T > T_{slew} \end{cases} \]  

where \( Q = C_1x + C_2V_r \) and \( x \) and \( V_r \) are the input and feedback reference voltages, respectively. \( V_r = \pm V_o \) depending on the digital output. \( \tilde{C} \) is equal to \( (C_1 + C_2 + C_t)/C_t \); \( \omega \) is equal to \( \tilde{\gamma}_m/C_{eff} \), where \( \tilde{\gamma}_m \) is the effective input transconductance. \( T \) is the total time period for integration (slewing plus settling). \( T_{slew} \) is the slewing period and is equal to \( (|Q| - C_{eff} \Delta V_{th})/I_s \), where \( I_s \) is the available output current during the slewing period and \( \text{sgn}(Q) \) is the signum function. The first expression in Equation 9 corresponds to pure settling while the second one corresponds to slewing followed by settling. The above expression can be rewritten by factoring out the \( Q/C_t \) term.

\[ \Delta V_o(T) = \begin{cases} \frac{Q}{C_t} (1 - \frac{\tilde{C} \Delta V_{th}}{|Q|} e^{-\omega T}) & \text{if } T < T_{slew} \\ \frac{Q}{C_t} (1 - \frac{\tilde{C} \Delta V_{th}}{|Q|} e^{-\omega(T - T_{slew})}) & \text{if } T > T_{slew} \end{cases} \]  

By comparing the above expression with Equation 6, we can obtain the general expression for \( K(x) \) shown below.

\[ K(x, V_2) = \begin{cases} 1 - \frac{\tilde{C} \Delta V_{th}}{|Q|} e^{-\omega T} & \text{if } T < T_{slew} \\ 1 - \frac{\tilde{C} \Delta V_{th}}{|Q|} e^{-\omega(T - T_{slew})} & \text{if } T > T_{slew} \end{cases} \]  

The first term on the right corresponds to the pure settling situation while the second term corresponds to the slewing followed by settling situation. The \( K \) factor shown above is a highly nonlinear function of the input signal and the feedback reference voltage. In accordance with the previous notation, \( K^+(x) = K(x, -V_r) \) and \( K^-(x) = K(x, V_r) \). For the second term in the equation shown above, it is important to notice that \( K(x, V_2) \) is only a function of the magnitude of the stored charge \( Q \) and is independent of the sign of this charge, i.e., \( K(-x, -V_2) = K(x, V_2) \). This observation leads to the following equations: \( K^+(-x) = K^-(x) \) and \( K^+(-x) = K^-(x) \) for \( x > 0 \), \( K^+(0) = K^-(0) \). Relating the above equations to Equation 8, we can obtain the analytical features of the nonlinearity error \( E(x) \): \( E^-(x) = -E^+(x), E(0) = 0, E(\pm 1) = 0 \). The asymptotic behavior of the function \( E(x) \) can be described as an odd symmetrical function with zeroes occurring at zero input, and the lower and upper limits of the input.

3.2 Analytical model

Pure settling only results in a gain error term which can easily be calibrated out. However, in general, for all practical situations the opamp in the modulator will experience both slewing and settling. We devote
our analytical model to this situation. Since the error curve has odd symmetry, without loss of generality, we only develop the model for $x > 0$. Around the error peak it can be shown that $K^+(x)$ can be approximated by one. The resulting error from this assumption is negligible. The expression of $K^-(x)$ can be written as

$$K^-(x) = 1 - \frac{\alpha}{1 + \hat{x}} e^{\alpha(\hat{x})}$$

where

$$\alpha = \frac{\dot{C} \Delta V_{th} C_1}{C_2 V_T}$$

$$\Omega(\hat{x}) = \omega \left( T - \frac{Q_m - Q_{th}}{I_s} \right)$$

and $Q_m = C_2 V_T (1 + \hat{x})$, $Q_{th} = C_{eff} \Delta V_{th}$. Plugging the above expression into Equation 8, we can get

$$E(\hat{x}) \approx \frac{\alpha (1 - \hat{x}) e^{\alpha(\hat{x})}}{2}$$

The peak error and location can be found by setting the first derivative of $E(x)$ to zero. The peak location turns out to be

$$\hat{x}_o = 1 - \frac{C_{eff}}{C_2} \frac{1}{V_T} \frac{I_s}{g_m}$$

where $\omega = g_m / C_{eff}$ has been used to derive the above expression. The expression can be further written as

$$\hat{x}_o = \begin{cases} 
1 - \frac{C_{eff} \Delta V_{gs}}{C_2} & \text{strong inversion} \\
1 - \frac{C_{eff} \Delta V_{gs}}{C_2} & \text{weak inversion}
\end{cases}$$

where $\Delta V_{gs}$ is equal to $V_{gs} - V_T$ of the input transistor. The error peak can be found to be

$$E(\hat{x}_o) = 2 \gamma e^{-\frac{\tau}{2}}$$

where

$$\gamma = \left( \frac{\Delta V \Delta V_{th}}{V_T^2} \right) \left( \frac{C_{eff} + C_1}{C_2} \right)$$

$$\tau = \frac{1}{\omega}$$

$\tau$ stands for the time constant of the opamp. The equation is for strong inversion. By replacing $\Delta V_{gs}$ by $2nU_T$, will result in the expression for weak inversion. Equation 18 shows that the height of the nonlinearity error is exponentially proportional to $-T/\tau$, where $T/\tau$ is the total number of the time constants in the integration period. As will be shown later, this is a testable conclusion which can be used to compare our model with experimental data. Additionally, it can be shown that the nonlinearity error in higher order $\Delta \Sigma$ modulators is dominated by the nonlinearity error in the first stage. Therefore, the analytical results developed here can be used to predict the opamp induced nonlinearity error for higher order converters as well.

**Figure 2: Simulation vs. model**

### 4 Experimental results

Our model has been validated via difference equation simulations and via measured results from fabricated ICs. First, we present simulation results. In Figure 2 we plot the nonlinearity error (output-input) vs. the input for a 2nd order modulator. The gray curve shows the results from difference equation simulations using MATLAB and the dark curve shows the results from our analytical model. As can be seen in the figure our analytical model and simulations results agree extremely well.

To further validate our results, a second order $\Delta \Sigma$ modulator was fabricated in a standard 0.8μm CMOS N-well process. The integrators in both the stages were autozeroed [8]. The settling behavior of the opamp is described by the number of settling time constants, $T_{settle}/\tau$. In our design, the nominal value of this number for the first opamp is around 14 which falls into the fast regime described in [5]. Since the length of the settling period $T_{settle}$ is designed to be equal to half of the total integration period $T$, the total number of time constants $T/\tau$ is then equal to 28. The input transistors are designed to operate in weak inversion. Therefore, the number of time constants is linearly proportional to the supply current. The modulator operates with a 5V supply voltage. A linear ramp from -80% to +80% of the input range is generated using a Wavetek 4808. The digital output is acquired via a National Instruments DIO-32F card.

According to Equation 18, if the supply current is reduced, so is the number of time constants. Therefore, the nonlinearity error is expected to increase exponentially. In our experiment, the supply current is set to six different settings of 0.25, 0.32, 0.40, 0.5, 0.65 and 1, where 1 corresponds to the nominal value. For each current setting, the nonlinearity error is measured. Figure 3 shows three sets of measured results.

We use three curves to visualize how the nonlinearity error progresses when the supply current is reduced. These curves preserve the main features: odd symmetry around the mid-point of the input signal, occurrence of error peaks and near zero error at midpoint and both ends. As the input devices continue to operate in weak inversion, the location of the error peak is independent of the supply current and is located around 0.5 which agrees with theoretical predictions.

As mentioned earlier, the height of the nonlinearity error is exponentially proportional to $-T/\tau$. Therefore, for input devices in weak inversion, we expect to see a straight line in a semilog plot of error height.
Figure 3: Measured nonlinearity error

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Figure 4: Current dependency of error height

vs. current. Figure 4 plots the maximum value of nonlinearity error vs. the supply current with the Y-axis being in log scale. As we can see the curve has two distinct regions. When the supply current is low (≤ 0.5), the nonlinearity error increases exponentially when the current is reduced. The inclined dashed line is the exponentially fitted curve. Since the X-axis represents the normalized supply current, the slope of the fitted line yields the number of time constants for the nominal supply current. The fitted slope is 27.935 which agrees very well with the design target of 28. In this region measurement fits the theory accurately. Please note that this extracted slope is independent of the total number of time constants for the second opamp. This observation justifies our assumption that the nonlinearity error is dominated by the nonlinear settling error from the first opamp. However, when the supply current increases, the nonlinearity error deviates from its exponential curve and starts to level off as shown by the horizontal dashed line. In another words, the nonlinearity error is limited by other nonlinear factors. One of the possible causes is capacitor nonlinearity due to the voltage dependence of the capacitor. A quick estimate can be carried out here. First-order voltage dependence is canceled due to the fully differential structure. Only the second order term is considered here. When normalized, the capacitor nonlinearity error in the fully differential ADC must be of the form αV ref 2, where α is the second order coefficient and in the range of 1-10 ppm [9]. It has a ballpark value of 10^-5 to 10^-4 and is supply current-independent. This value agrees reasonably well with Figure 4. Figure 4 suggests that the nonlinearity error is usually limited by factors other than nonlinear settling for larger currents. The conventional wisdom where we use a large supply current to limit the nonlinear settling distortion is not effective and this extra power is wasted. We can see from the figure that for our nominal design a 40 percent power reduction does not increase nonlinearity error.

5 Conclusions
In this paper, we have established a mathematical framework to analyze the nonlinear behavior in ΔΣ modulators. Though the framework is general and can be extended to model other nonlinear effects, in this paper we restrict ourself to analyze the nonlinear settling behavior in ΔΣ modulators. The model utilizes only the device parameters, which allows designers to optimize the circuit performance. Our model was validated using simulation and fabricated designs. A second order ΔΣ modulator was fabricated to demonstrate the validity of our theory. Measurement results suggest that for higher currents nonlinearity is dominated by voltage-dependent capacitor nonlinearity. Using our model a 40% reduction in power consumption did not result in increased nonlinearity.

References