An Ultra Low Power Transconductance Cell

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Abstract
This paper describes an implementation of a linear programmable transconductance cell with low distortion and bias currents in the range of 100nA - 300nA. The power dissipation is approximately 1.5μW at 3V supply for a 2Vp-p input range and approximately 900nW at 3V supply for a 1Vp-p input range. The total harmonic distortion (THD) is -42dB for a input voltage of 2Vp-p. The programmable transconductance cell can be tuned by varying its bias currents. Simulation and experimental results have been used to confirm its operation.

1 Introduction
There has been substantial research done in the area of adaptive filters. Adaptive filters find applications in a number of areas including biomedical instrumentation, acoustics, control systems, etc. A particular application of interest is reducing acoustic feedback in hearing aids using an adaptive filter. A method utilizing a filter bank of over 25 programmable filters has been proposed previously for hearing aids [8]. Because of limited size and portability, this application requires that the entire filter bank fit on a single chip and consume extremely low power. Traditionally, continuous time filters are used for high frequency applications. However, here we use it for very low frequency applications (i.e. 100Hz - 5KHz) and exploit its small size. Unlike switched capacitor circuits, adding programmability does not increase on-chip area [1, 2]. In switched capacitor circuits adding programmability involves adding capacitor banks. While in continuous time transconductance-C filters adding programmability involves adding a single set of references which can be shared by a number of filter cells.

There are a number of different approaches for the implementation of continuous time integrated filters. Most commonly they use either the square-law characteristics of MOS transistors [3] or the degenerated transconductance of the differential input gate stage [4, 5]. In this paper a fully differential programmable transconductance filter is presented. The tuning of the filter is accomplished by altering the bias currents. A master-slave technique is used to compensate for process variations [5]. The primary feature of this amplifier is that it consumes extremely low power while providing a fairly large linear range.

The rest of the paper is organized as follows. The design of a transconductance cell is presented in Section 2. Simulation and experimentally measured results supporting the design is discussed in Section 3 and finally, we end with some conclusions in Section 4.

2 Circuit Design
In this section we describe the programmable linear transconductance cell along with factors affecting its range and tunability ability.

Basic transconductance-C cell The basic concept of a continuous time transconductor-C filter cell is illustrated in Figure 1. The transconductance element produces a differential output current that is linearly proportional to the differential input voltage \( V_{in} \). The output current \( I_{out} \) is integrated by the capacitor \( C \), to yield the transfer function shown in equation 1. This forms a first order low pass filter and forms the basis for all higher order filters.

\[
H(s) = \frac{Gm}{sC} \quad (1)
\]

The proposed structure for the linear transconductance cell is shown in Figure 2. Cascoding transistors \( M_2 \) and \( M_4 \) are operated in the saturation region in weak inversion to obtain high transconducance at low currents. Transistors \( M_3 \) and \( M_5 \) are operated in the triode region in strong inversion to provide the largest linear range. The cascoding transistor \( M_2 \) combined with auxiliary opamp \( E_2 \) provides a constant \( Vds \) across \( M_1 \) and the cascoding transistor \( M_4 \) combined with auxiliary opamp \( E_2 \) provides a constant \( Vds \) across \( M_3 \). The analysis of the circuit
Figure 2: Linear transconductance cell

Figure 3: Input transistors and small-signal model

is as follows. Since the circuit is symmetrical we shall consider only the left half of the circuit. The equations for $M_1$ operated in triode and strong inversion are shown in equations 2 and 3

$$I_{ds1} = \beta(V_{gs1} - V_T - \frac{V_{ds1}}{2})V_{ds1}$$

(2)

$$g_{m1} = \frac{\partial I_{ds1}}{\partial V_{gs1}} = \beta V_{ds1}$$

(3)

Therefore, the transconductance of transistor $M_1$ depends only on $V_{ds1}$. Now considering the input and its small signal model shown in Figure 3 we can write the expression for the effective $g_m$ shown in equation 4

$$g_m = \frac{\partial I_1}{\partial V_{1}} = \frac{-g_{m1}(g_{m2} + g_{m2}A + gds2)}{g_{m2} + A g_{m2} - gds1 - gds2} \approx -g_{m1}$$

(4)

Therefore for large enough gain the transconductance of the overall input circuit primarily depends on the transconductance of the input differential transistor $M_1$.

The constant voltage source $V_b$ is implemented as shown in Figure 4. $M_5$ is operated in triode and $M_6$ in saturation, transistor $M_5$ is designed to be longer than $M_6$.

**Linear range**: We now describe the linear range for the circuit in Figure 2. The equation for $M_1$ in the triode region can be rewritten in the form as shown in equation 5.

$$\delta V = (V_{gs} - V_T) = \frac{I_{ds}}{\beta V_{ds}} + \frac{V_{ds}}{2}$$

(5)

Now let us consider two cases:

Case 1: Differential input voltage is equal to zero.

$$I_{dsm1} = \frac{I_b}{2}$$

(6)

$$\delta V_{m1} = \frac{I_b}{2 \beta V_{dsm1}} + \frac{V_{dsm1}}{2}$$

(7)

Case 2: Differential input voltage is at its maximum.

$$I_{dsm1} = I_b$$

(8)

$$\delta V_{m1} = \frac{I_b}{\beta V_{dsm1}} + \frac{V_{dsm1}}{2}$$

(9)

The linear range of the transconductance cell is equal to twice the difference between the maximum and the minimum values calculated above and is shown in equation 10.

$$\delta V = \frac{I_b}{2 \beta V_{ds}}$$

(10)

Thus the factors affecting the range are the tail current $I_b$ and drain to source voltage of transistor $M_5$. Additionally, from equation 3 we note that the transconductance is a function of $V_{dsm1}$. However, because of the auxiliary opamp $E_{q1}, V_{dsm1}$ is equal to $V_{dsm5}$. Therefore, if we are to keep a constant linear range while altering the transconductance (by varying $V_{dsm5}$) we have to vary $I_b$ proportionately. Though, $V_{dsm}$ is a nonlinear function of the current.
In $Ib2$, it can be linearized around an operating point such that $Vds2 \approx \kappa Ib2$, where $\kappa$ is a constant. Therefore, the transconductance can be programmed while maintaining a constant linear range by varying both $Ib$ and $Ib2$. The linearity of this relationship is not critical when the filter includes a master slave tuning scheme. Its primary impact is a change in the linear range with different transconductance settings.

The circuit diagram for the complete transconductance cell complete with the auxiliary opamp circuits is shown in Figure 5. For our design example we have selected a filter frequency of $2KHz$ and a capacitor size of $10pF$. This results in a transconductance of approximately $0.06\mu A/V$. Using a $Vds$ of $70mV$ for $M1$ gives us a $W/L$ ratio of $1/100$ for $M1$. The drain to source voltage of $70mV$ was chosen as a compromise between linear range and immunity to random offset voltages. It can be shown that for a given pole frequency and linear range, the minimum theoretical tail current is given by equation 11, where $f0$ is the pole frequency and $C$ is the capacitance. For our set of conditions $I_{min} \geq 125nA + Ib2$. We choose a tail current of $200nA$. A $V_T$ mismatch of approximately $10mV$ did not change the transconductance appreciably and the linear range was not affected. The design for a fully differential transconductance cell is shown in Figure 6. Self bias cascode current mirrors are used to increase the gain of the circuit [9].

$$I_{min} = \frac{2\pi C f_0 \delta V}{2}$$

(11)

The transconductance cell can be used as a slave in the master-slave configuration of an adaptive filter to tune the frequency and quality factor. The master-slave tuning strategy is an automatic tuning scheme which is used to guarantee accurate performance of continuous time filters [7]. The master models with precise accuracy the performance of the slave and then applies a corrective reference signals (in our case the currents $Ib$ and $Ib2$) to both the master and the slave simultaneously.

3 Results

In this section we provide simulation and measurement results. For both simulation and measurements the currents $Ib$, $Ib2$ and $Ib3$ are set at $200nA$, $34nA$ and $34nA$ respectively and the supply voltage is $3V$. The auxiliary opamps $E1$ and $E2$ have a gain of $63dB$ for a tail current of $50nA$. All measurements are done on a $HP4155A$ parameter analyzer.

First we present the simulation results. In the first experiment, we illustrate the programmability of the transconductance cell by varying the bias currents. The results are shown in Figure 7. In this experiment the bias current ($Ib$) is varied from $100nA$ to $300nA$. The range is kept constant by varying the Vds of transistor $M5$ which in turn is varied by controlling current $Ib2$. In this experiment $Ib2$ is varied from $20nA$ to $80nA$ in steps of $20nA$. As we note in Figure 6 the linear range is constant for the different values of transconductance.

In the second experiment we plot the THD versus the input voltage magnitude as shown in Figure 8. The input signal amplitude is plotted on the X axis in linear scale and total harmonic distortion is plotted on the Y axis in log scale. We note that the THD is $-42dB$ for an input amplitude of $1V$, (i.e. $2V_{pp}$).

Figure 9 shows the measured differential output current versus input voltage for the fabricated integrated chip. The tail current is set at $200nA$ and current $Ib2$ is set at $34nA$. We note that the linear range is approximately $2V_{pp}$ with an input referred offset voltage of $2mV$.

4 Conclusions

A novel continuous time linear tunable transconductance cell has been described. The linear voltage range of the circuit is varied by controlling the tail currents. Power dissipation is $900nW$ at $3V$ supply for a $1V_{pp}$ input range and $1.5\mu W$ at $3V$ supply for a $2V_{pp}$ input range. Power consumption can be further reduced by lower the tail currents of the auxiliary opamps and providing a non-unity gain factor.
for the current mirrors. We expect the total power to be reduced to a third of its current value. The proposed transconductance cell is suitable for the design of large filter banks of programmable filters because of its small size and low power consumption. THD is $-42\,dB$ for an input voltage of $2V_{p-p}$. Simulation results and measurements from a fabricated design in a MOSIS 2$\mu$m N-well CMOS process were used to verify its operation.

References


