Digital Detection of Parametric Faults in Data Converters

Bapiraju Vinnakota and Ramesh Harjani
University of Minnesota, Minneapolis, MN 55455

Abstract

Multiple parametric faults due to normal process variations are extremely important for analog circuits. Very few analog DFT techniques target multiple parametric faults. In this paper we present a DFT scheme that targets high performance analog circuits. In particular, we target a popular switched-capacitor based A/D converter. The DFT scheme is based on an analog-to-digital capacitor ratio converter circuit. The circuit is used to completely characterize the transfer function of a charge redistribution A/D converter. Extensive simulation results that include practical process variations are used to verify our DFT scheme.

1 Introduction

The I/O relationship of a manufactured data converter may differ from the ideal because of isolated manufacturing errors causing local physical defects and more importantly because of parametric deviations caused by normal process variations. Large deviations can be detected by tests that target physical defects. A collection of minor deviations, may be a fault in that it alters the functionality of a device. As they have higher frequency than single large deviations, multiple parametric faults are more important in analog ICs. Since the set of multiple parametric faults cannot usually be enumerated fault-oriented test techniques cannot effectively detect multiple parametric faults. Therefore, test techniques for practical converters, usually based on device specifications, verify that the I/O relationship of the circuit under test and a manufactured converter is close to the stairstep desired in ideal converters. The specifications tested for include the offset, gain, integral nonlinearity (INL), and differential nonlinearity (DNL) errors [1]. Researchers have developed a variety of design for test schemes for data converters based primarily on calibration techniques [2] and data encoding [3, 4]. Though they are effective at detecting significant single faults they are ineffective at detecting multiple parametric faults. In all cases either the fault coverage is low or number of good circuits which fail the test is unacceptably high. Sigma-delta converters have also been used to digitally generate accurate signal sources for BIST schemes for several circuits including data converters [5]. Readers are referred to [6] for more details. We develop a design for test technique based on digitally measuring on-chip capacitor ratios. The measurement can be used to digitally characterize the I/O transfer function of the circuit under test. First, we discuss the converter targeted by our test technique.

2 Data Converter Architecture

The charge redistribution A/D data converter, shown in Figure 1, consists of a set of capacitors, switching circuitry and a comparator. To produce an n-bit output, the total capacitance required is \(2^n C_{\text{unit}}\) (\(C_{\text{unit}}\) is a “unit” capacitance), distributed over \(n\) capacitors of sizes \(C_{2n-1}, C_{2n-2}, \ldots, C_2, C_1\) and \(C_0\) (\(C_0\) refers to a capacitor of size \(2^n C_{\text{unit}}\)). The converter produces the best digital match for the analog input with an iterative search of the space of \(2^n\) potential values. On each iteration, the search space is bisected and the search narrowed to one of the two halves. One output bit is computed on each iteration in descending order from the most significant output bit. The arithmetic required is performed by redistributing the charge stored on the capacitors. The redistribution alters the voltage at the negative input, which we will refer to as \(V_n\), to the comparator. Conversion also requires a reference voltage \(V_{\text{ref}} = 2^n V_{\text{step}}\), where \(V_{\text{step}}\) is the analog voltage corresponding to 1 LSB. Initially, \(V_n\) is set to \(V_{\text{ref}}\). In the first step, charge is redistributed by switching one terminal of the capacitor \(C_{2n-1}\) [7] such that \(V_n\) drops to \(V_{\text{ref}} / 2\). If \(V_n > 0\), then the most significant bit (MSB) is set to 1. Else, it is restored to its previous value by reversing the redistribution and the MSB is reset to 0. In general, in iteration \(i, i = n - 1\) down to \(i = 0\): A voltage of \(V_{\text{step}} / 2^{i+1}\) is subtracted from \(V_n\), by redistributing charge by switching one terminal of the capacitor \(C_{2i}\). If \(V_n > 0\), then bit \(i\) is set to 1 and conversion proceeds; Else if \(V_n \leq 0\), then it is restored by reversing the redistribution, bit \(i\) is reset to 0 and conversion proceeds.

3 Ratio-Based Fault Detection

Ideally, the converter I/O transfer function should be a stairstep function. The height of each step is 1 LSB and its width should be \(V_{\text{step}}\). We will refer to the input voltages at which the digital output changes by 1 LSB.
as transition voltages. Each such change will be referred to as an output transition. The position of each transition is determined by the ratios of component capacitances to the total capacitance \( C_{\text{total}} \). For example, the position of the transition at the midpoint of the input range, at a voltage equal to \( \frac{V_{\text{ref}}}{2} \), is determined by the ratio \( \frac{C_{4}}{C_{\text{total}}} \). Each capacitor ratio determines a single bit in the output. A transition to the digital output vector \( d_{n-1}d_{n-2} \ldots d_{1}d_{0} \) is determined by the ratios corresponding to the bits which are at 1 in the vector. We develop a DFT technique for the charge redistribution converter based on measuring these on-chip capacitor ratios.

### 3.1 Fault analysis

Multiple parametric faults may occur in either the active or passive components of the system. In any switched capacitor circuit, the passive components, the capacitors, occupy a far larger fraction of system area than the active components. Hence, we focus on detecting multiple parametric faults in them. It is possible, though not guaranteed, that our test technique will also detect many multiple parametric faults in the active components. We represent the impact of faults as deviations of the capacitances from their expected values. Faults will cause the ratios of individual capacitances to the total capacitance to deviate from their expected values. This will affect the location of one or more transitions in the I/O transfer function. First, we consider the impact of a single ratio fault.

**Single fault analysis:** For a single ratio fault, we assume the ratios of all capacitors (to the total capacitance - hence, we will not state this phrase explicitly) but one are at their expected values. (This construct is purely hypothetical since an error in the value of even one capacitor will cause a multiple ratio fault.) Working with a specific example will be useful. Consider a 3 bit data converter with a total capacitance of \( C_6 \) distributed among four capacitors of sizes \( C_4, C_2, C_1 \) and \( C_1 \). The three capacitor ratios used for conversion are \( \frac{C_4}{C_6}, \frac{C_2}{C_6} \) and \( \frac{C_1}{C_6} \). Assume the ratio \( \frac{C_4}{C_6} \) is not exactly equal to half. That is \( \frac{C_4}{C_6} = 0.5(1 + \epsilon_4) \), where \( \epsilon_4 \) may be positive or negative. Clearly, the transition 100 will be affected by this fault. Instead of occurring at \( V_{n} = \frac{V_{\text{ref}}}{2} \), it will occur at the input voltage \( V_{n} = \frac{V_{\text{ref}}}{2}(1 + \epsilon_4) \). This will not be the only transition affected by this fault. The transition 110 should occur at the input voltage \( V_{n} = \frac{5}{8}V_{\text{ref}} \). In the presence of the fault it will actually occur at the input voltage \( V_{n} = \frac{5}{8}V_{\text{ref}}(1 + \epsilon_4) \). Every transition in which the most significant bit is 1 is affected by the fault. The shift in the absolute input voltage for the transition is equal to \( \frac{V_{\text{ref}}}{2}\epsilon_4 \). If the input voltage is less than \( V_{n} = \frac{5}{8}V_{\text{ref}}(1 + \epsilon_4) \), the original voltage \( V_{n} \) is restored by reversing the charge redistribution. Any errors in the \( V_{n} \) introduced by the ratio fault are eliminated. Thus, none of the transitions for which the most significant bit is 0 will be affected by this fault.

### Table 1: Ideal and actual transitions for a multiple ratio fault

<table>
<thead>
<tr>
<th>Tran to</th>
<th>Ideal Volt.</th>
<th>Actual Volt.</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_1) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_1) )</td>
</tr>
<tr>
<td>010</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
</tr>
<tr>
<td>011</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_1) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_1) )</td>
</tr>
<tr>
<td>100</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_4) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_4) )</td>
</tr>
<tr>
<td>101</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
</tr>
<tr>
<td>110</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_4) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_4) )</td>
</tr>
<tr>
<td>111</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
<td>( V_{\text{ref}}/2 ) ( (1 + \epsilon_2) )</td>
</tr>
</tbody>
</table>

The analysis can be generalized to an \( n \)-bit converter. Let \( \epsilon_i \) refer to a relative error in the ratio \( \frac{C_i}{C_{\text{total}}} \), \( 0 \leq i \leq n - 1 \). That is instead of \( \frac{1}{2} \), it is actually \( \frac{1}{2} (1 + \epsilon_i) \). This error will affect all transitions for which bit \( i \) is set to 1. Because the voltage \( V_\ell \) is restored on every transition for which bit \( i = 0 \), none of the transitions in which bit \( i = 0 \) are affected by the fault. The shift in the input voltage for all the transitions affected by the fault will be \( \frac{V_{\text{ref}}}{2 \cdot 2^i} \epsilon_\ell \).

**Multiple fault analysis:** The analysis of the impact of multiple faults is a direct extension of the above analysis. The bisection operations performed by each of the ratios are independent of one another. Therefore, the errors produced by faults in the individual ratios are also independent of one another. The errors produced by the individual faults will simply be linearly superposed. A fault in the \( i^{th} \) ratio \( \frac{C_i}{C_{\text{total}}} \) will affect all the transitions in which bit \( i = 1 \). For the multiple faults in the \( i^{th} \) and \( j^{th} \) ratios, errors produced by the two will simply be added for all the transitions in which bit \( i = j = 1 \). The error in the input voltages induced by the ratios (for these transitions) is \( \frac{V_{\text{ref}}}{2^i} \epsilon_\ell + \frac{V_{\text{ref}}}{2^j} \epsilon_\ell \). The errors induced by any multiple ratio fault can be similarly calculated. Given an arbitrary multiple fault, the I/O relationship of the faulty data converter can be completely characterized. The characterization can be used to estimate the various errors of interest such as the offset, gain, DNL and INL errors. For the 3-bit converter, let the errors in the three ratios of interest be \( \epsilon_4, \epsilon_2 \) and \( \epsilon_1 \) respectively. The transition voltages in the good and faulty converters are shown in Table 1. As expected, errors in the significant ratios have a relatively greater impact on the transition voltages.

### 3.2 Test Technique

Given a circuit to be tested, if all the capacitor ratios of interest can be measured, their deviations from the desired values is known. Consequently, the transfer function of the circuit under test can be completely characterized. The characterization can be used to determine if the converter is acceptable. This is the approach we use in our DFT scheme. The quality of the characterization depends on the accuracy with which the ratios are measured. In the next section we develop a circuit which will digitally estimate all the ratios \( \frac{C_i}{C_{\text{total}}} \), \( 0 \leq i \leq n - 1 \), of
interest.

4 Design Example

In this section we provide circuit details for the analog-to-digital capacitance ratio converter (ADCRD). We show an example charge redistribution converter design and study the impact of single and multiple faults. And finally we provide simulation results to verify our DFT scheme.

ADCRD: The ADCRD circuit is able to accurately convert a capacitor ratio into a digital value. It can be shown that the average digital value [8] of the output is given by equation 1.

\[ V_{\text{digital-average}} = \frac{1}{n} \sum_{i=0}^{n-1} D_0(i) = \frac{C_a}{C_b} - \epsilon_n \]  

(1)

where \( C_a/C_b \) is the capacitor ratio desired and \( \epsilon_n \) is the error in the conversion process and is bounded by equation 2.

\[ \epsilon_{n_{\text{max}}} = \frac{2}{n} \left[ 1 + \frac{C_a}{C_b} \right] \]  

(2)

The set of equations above are valid for \( C_a \leq C_b \), with the result the error can always be bounded by \( 4/n \) and can be made extremely small by increasing the value of \( n \), i.e., the time spent on converting the capacitor ratio into a digital format.

Modified ADCRD: However, the simple ADCRD circuit introduced above cannot be used for values of \( C_a \geq C_b \). In the case of the charge redistribution converter, shown in Figure 1, the first ratio of interest is \( C_b/(C_b + C_a + C_2 + C_{1a} + C_{1b}) \). As the same capacitor cannot both be in the forward and feedback path of the ADCRD we consider an alternate ratio \( C_b/(C_2 + C_1a + C_1b) \) from which the original ratio can be derived. For this ratio, ideally both values should be matched perfectly. However, due to normal process variations both are going to be perturbed slightly from their ideal values. As we do not have any a priori knowledge we are unable to predict if the ratio is larger or smaller than unity. As pointed out earlier the basic ADCRD circuit is only capable of providing accurate ratios that are less than or equal to one. Therefore, a slightly modified version of the basic ADCRD circuit needs to be employed for this first conversion. The modified circuit is shown in Figure 2. It can be shown that the average digital value in this case is given by equation 3 and the error is again bounded by equation 2. Here for our example 3bit converter \( C_a \) represents \( C_8 \) and \( C_b \) represents \( (C_1 + C_2 + C_{1a} + C_{1b}) \).

\[ V_{\text{digital-average}} = \frac{1}{n} \sum_{i=0}^{n-1} D_0(i) = \frac{C_a}{C_a + C_b} - \epsilon_n \]  

(3)

There are a number of features of this circuit. First it was designed to have minimum impact on the operation of the normal data converter. That means limited circuit changes and any impact on performance should be benign. A comparison of the modified ADCRD circuit shown in Figure 2 and the circuit for the normal charge redistribution converter shown in Figure 1 shows the addition of two switches at the virtual ground of the opamp and an additional feedback capacitor. During normal operation one switch is permanently on and the other is permanently off. As MOS switches have zero offset the only impact of an open switch is a very small parasitic capacitance at the virtual ground node. The impact of parasitic capacitance on the virtual ground node is only a slight alteration in the gain error. As the nominal bottom-plate parasitic capacitance is usually large the impact of this additional switch parasitic should be completely negligible. To reduce the number of changes to the basic topology we have used the backward-Euler switched-capacitor implementation. Additionally, the impact of channel charge injection is the same in our modified ADCRD as in the original charge redistribution data converters.

Simplified modified ADCRD: For measuring all the other ratios \( C_i/C_{\text{total}}, i = 4 \ldots 1 \) a simplified version of the modified ADCRD circuit shown in Figure 2 can be used. The simplified circuit is shown in Figure 3. This circuit accomplishes the original goal of reducing the number of the modifications to the original data converter circuit and has a slightly simplified clocking scheme in comparison to the circuit shown in Figure 2.

5 Results

To validate our DFT technique and to evaluate the practical accuracy desired of the ADCRD we developed a
simulator for an N-bit converter. Gaussian distribution with appropriate variances and means are assumed for the capacitor sizes. The simulator accommodates both uncorrelated and correlated capacitor variances [9]. The simulator was developed using MATLAB.

Exp 1: In the first experiment we used a 4 bit data converter for visual clarity. The capacitors in this converter have multiple gross variations from their nominal values. The results are shown in Figure 4. The dotted straight line shows the code center of an ideal data converter neglecting gain and offset error. The dashed line shows the actual transfer function for this converter. And the solid line shows the transfer function predicted using an AD-CRC circuit with 1/4 LSB resolution. Here we note the good match between actual and estimated transfer functions. Our simulation results for data converters with 4bit to 14bit resolution suggest that 1/4 LSB accuracy for the AD-CRC is sufficient. As the successive approximation data converter is based on capacitor matching and the AD-CRC is not, obtaining 1/4 LSB accuracy using the AD-CRC circuit should not be a problem.

Exp 2: In the second experiment we provide results from Montecarlo runs. For this experiment a 4bit, a 7 bit and a 10 bit converter were used. The unit capacitor size was set to 0.5pF resulting in 0.2% matching for a 1:1 and progressively worse for other ratios [9]. Three hundred converter designs were generated. The capacitance matching for each of these converters followed a Gaussian distribution. Using our knowledge of the capacitor sizes, the actual transfer function was generated for each converter. The DNL from the actual transfer function was used to classify each circuit as good or faulty. A data converter with a DNL greater than 1LSB is considered to be faulty. Additionally, our AD-CRC circuits were used (via simulation) to extract capacitor ratio estimates. These estimates were then used to derive the estimated transfer functions. The estimates were used to declare the converter as having passed or failed the test process. A converter with an estimated DNL greater than 1LSB failed the test. The results are shown in Table 2. Here the probability of good is the initial yield, good fail is the probability that a good circuit erroneously fails the test and the fault coverage has the normal definition. We note that very few errors are made for an AD-CRC resolution corresponding to 1/4 LSB. We also note that the performance remains roughly the same for higher resolutions as well. Notice that the primary impact of increasing the resolution of the AD-CRC is a sharp decrease in the number of good circuits which erroneously fail.

<table>
<thead>
<tr>
<th>Conv Bits</th>
<th>ADCRC Resol.</th>
<th># of Runs</th>
<th>Prob.</th>
<th>Good</th>
<th>Fail</th>
<th>Fault Cov.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2 LSB</td>
<td>300</td>
<td>88.33%</td>
<td>79.7%</td>
<td>97.3%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1 LSB</td>
<td>300</td>
<td>87.33%</td>
<td>34.3%</td>
<td>79.3%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1/2 LSB</td>
<td>300</td>
<td>88.7%</td>
<td>5.3%</td>
<td>97.7%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1/4 LSB</td>
<td>300</td>
<td>87.0%</td>
<td>1.7%</td>
<td>99%</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1/4 LSB</td>
<td>300</td>
<td>89.2%</td>
<td>1.4%</td>
<td>99%</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>1/4 LSB</td>
<td>300</td>
<td>87.3%</td>
<td>2.3%</td>
<td>99%</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Montecarlo simulation results

6 Conclusions

We developed a DFT scheme for the large number of analog circuits that rely on capacitor ratios. Our analysis focused on charge redistribution A/D converters. We showed that one can completely characterize the I/O transfer function of a converter by measuring all capacitor ratios in it. We developed a circuit that digitally estimates all the ratios of interest in the target converter. The values generated by the digital estimator can be used to reach a decision on the quality of the circuit under test. Our results showed that for an estimator resolution of 1/4 LSB, the accuracy of our scheme is greater than 97%. We believe this is the first DFT method to demonstrate such effectiveness at detecting parametric faults.

References