A TELEMETRY AND INTERFACE CIRCUIT FOR PIEZOELECTRIC SENSORS

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ABSTRACT

In this paper we present a design for a two-wire telemetry and signal conditioning circuit for piezoelectric sensors. The telemetry system uses an on-chip voltage regulator as part of the signal-vs-supply filter. We also introduce a new shielded-base bipolar opamp design that exploits the properties of both MOS and bipolar transistors. The new design results in 10X reduction in power for a 10dB reduction in signal-to-noise ratio. For this design the bandwidth of interest is 10kHz to 1MHz and the sensor capacitance size is 100pF.

1. INTRODUCTION

Sensors and sensor interfaces allow us to interact with real world signals. Increasingly, sensors are now being used with micromachined techniques with integrated circuit components [4]. In this paper we describe a CMOS interface circuit for a piezoelectric acoustic emission sensor and the necessary telemetry circuits to provide the signal externally. This sensor is intended to be used to detect acoustic emission that are precursors to catastrophic failures in military equipment [2, 3]. The primary objective is to develop real-time sensing devices and methods to accurately identify conditions leading to the imminent failure of critical aircraft components. The two important technologies brought together for this purpose are microsensors and sensor conditioning electronics. The microsensor used is a thin film acoustic emission (AE) sensor which detects the development of cracks and unusual wear in the body of aircrafts and submarines. The signal conditioning electronics is used to identify and amplify the signal from the acoustic emission microsensor within an electrically and acoustically noisy environment. The other goal of this project is to realize inexpensive and low power silicon chips which can be distributed over critical regions of the aircraft or submarine. To realize this goal it becomes necessary to implement the complete system with a minimum number of external wires and components. We use a two-wire system for both power delivery and telemetry. A block diagram for the complete system is shown in Figure 1.

The microsensor used is a piezoelectric thin film because of its high reliability, superior performance and small area. A piezoelectric sensor acoustically coupled to an aircraft component is shown in Figure 2. The magnitude of the output signal from the microsensor is proportional to the magnitude of the outgoing ultrasonic waves from any acoustic emission event. The design and fabrication of thin film piezoelectric microsensors is beyond the scope of this paper. However, a microphotograph of the integrated AE sensor to be used with our circuit is shown in Figure 3.

The signal bandwidth of the acoustic emission signals vary from about 10 KHz to about 1 MHz. Mixed in with the desired acoustic emission signal is vibration and fretting noise due to the mechanical parts. However, this noise is limited to about 10 KHz and can be filtered out. We exploit this frequency differentiation to perform telemetry, and supply power to the signal conditioning circuits along the same two wires. Power is supplied to the remote sensor and signal conditioning circuitry via two wires. The amplified sensor signal is carried back along the same two wires that are used to supply the power to the sensor interface. To accomplish this two-way power and data transmission an on-chip filter and power supply are required. The complete systems consists of a small discrete external interface and an integrated circuit that consists of an on-chip power supply, a charge amplifier, a voltage amplifier and an integrated piezoelectric sensor.

Signals from the integrated piezoelectric acoustic emission sensor are first amplified via a charge amplifier. Further amplification is accomplished using a voltage amplifier. We use a charge amplifier to interface to the sensor for a number of reasons. First, the charge amplifier is not affected by parasitic capacitances associated with the sensor or at the input of the amplifier. Second, the output voltage of our piezoelectric sensor is very small. This is because of the high dielectric constant of PZT [1], which is the piezoelectric material used. However, we use PZT as our sensor material because of its extremely high piezoelectric constant. A voltage amplifier was designed for some additional gain and a buffer circuit was added between the charge amplifier and the voltage amplifier for impedance matching.

The rest of the paper is organized as follows. The design of the telemetry and signal conditioning circuits are discussed in Section 2. Simulation and measurement results confirming the operation of these designs is discussed in Section 3. And finally, we provide some conclusions in Section 4.
2. CIRCUIT DESIGN

In this section we describe the circuit designs for the telemetry and signal conditioning circuitry. In particular we provide detailed designs for the power regulator and telemetry circuitry and the charge and voltage amplifiers. First we discuss the power regulator and telemetry circuits.

2.1. Power regulator and telemetry

The operation of the power regulator and telemetry circuitry is best understood with the help of the simplified circuit shown in Figure 4. Here $V_e$ is the external power supply. $L_d$ and $R_d$ form the external discrete inductor. $R_d$ is the parasitic series resistance of the inductor. $R_e$ is a damping resistor to critically dampen the second order resonant system that is formed. $E_1$ is an external high-gain low noise amplifier. The amplified sensor signal is capacitively coupled via $C_r$ to the single signal-power line. With the help of the capacitor $C_i$, the external amplifier $E_1$ provides an AC virtual ground at the common signal-power wire. An AC signal is directly coupled and amplified to generate the external sensor signal. The inductor $L_d$ provides an AC open for the AC sensor signals and provides a DC short to the power being supplied to the chip. The damping resistor $R_e$ is used to avoid oscillations. If the parasitic series resistance is assumed to be small and the damping resistor is assumed to be large then it can be shown that the signal transfer function from RHS of $C_r$ to the output is given by equation 1.

$$\frac{V_{out}}{V_{in}} = \frac{s^2 L_d C_r}{1 + s^2 (C_o + C_e) L_d}$$  \hspace{1cm} (1)

$$f_0 = \frac{1}{2\pi \sqrt{L_d (C_o + C_e)}}$$  \hspace{1cm} (2)

If we assume that $C_e \ll C_o$, then for frequencies greater than $f_0$ shown in equation 2, the transfer function is given by $C_e/C_o$, which is just a fixed gain.

The in band noise transfer function of the external amplifier is given by equation 3 in our signal band. For typical component noise of the external amplifier is amplified, thereby mandating an extremely low noise amplifier. It is possible to meet the design specification of approximately 60dB SNR with an appropriate choice of amplifier.

$$H_\text{n}(s) = \frac{C_e}{C_o L_d s}$$  \hspace{1cm} (3)

An AC variation in the power consumption cannot be distinguished from the signal. Therefore, it is necessary to maintain as constant a power consumption for the signal conditioning circuitry as possible. To this end as shown later, all the designs for the amplifiers use constant current topologies, i.e., class A.

2.2. Signal conditioning circuitry

Next, we consider the circuits used to amplify the sensor signals [5, 6]. A simplified circuit diagram for the signal conditioning circuit is shown in Figure 5. The inverting terminal of the operational amplifier is at virtual ground and therefore any charge that is generated across the sensor flows into the feedback capacitor $C_f$. The voltage gain of the circuit is given by the ratio of $C_e$, where $C_e$ is the sensor capacitance, over $C_f$. Hence to obtain high gain, $C_f$ must be made much smaller than $C_e$. This basic topology has a number of limitations including low frequency flicker noise of the amplifier, operational amplifier offset and long term drift. Traditionally, correlated double sampling and chopper stabilization are used to remove low frequency noise and offset. However, our signal band does not include the frequencies from DC to 10KHz. Additionally we do not have a clock signal available to us which is necessary for both correlated double sampling and chopper stabilization. Hence a resistor, $R_f$, connected across the feedback capacitor is used as a low frequency feedback path to reduce the effect of low frequency noise and offset. The transfer function of the charge amplifier circuit is now given by equation 4.

$$\frac{V_o}{V_{in}} = \frac{-R_f C_e s}{1 + R_f C_f s}$$  \hspace{1cm} (4)

In our design the gain of the charge amplifier is selected to be 20dB for a number of reasons, therefore we include a voltage amplifier for additional gain. The amplifier design is a simple two stage Miller compensated OTA design with a compensation capacitor of 5pF and total power compensation of about 100nW. The
voltage amplifier circuit has a gain of 10 which is obtained by using resistor ratios. The same amplifier is also used as a buffer between the charge and the voltage amplifier for impedance matching. In the next paragraph we introduce a novel shielded-base BiCMOS operational amplifier for the charge amplifier stage.

2.3. Shielded-base opamp design

The complete transistor level circuit diagram for the shielded-base opamp is shown in Figure 6. The transconductance for bipolar transistors is proportional to the current while the transconductance for MOS devices is proportional to the square root of current. Therefore, as is shown below, the power savings from using a bipolar input differential pair can be substantial. However, in our charge amplifier application it is necessary to maintain zero input current. Therefore, we use MOS devices (M1 and M2) to shield the base of the bipolar transistors (B1 and B2). The bipolar transistors provide the transconductance while the MOS transistors, used as source followers, provide infinite input impedance.

Next, we compare our design with traditional designs in terms of power and noise. Let us first consider power. We compare our design with a traditional MOS only input pair. For MOS transistors operated in strong inversion the minimum power requirement is given by equation 5.

$$ P = V I = \frac{V (2 \pi BW C)^2}{2 kT C} $$

where, BW is the bandwidth, C is the sensor capacitance, $kT$ is the transconductance factor and $W/L$ is the aspect ratio of the transistor. On the other hand, the minimum power requirement for bipolar transistors is given by equation 6.

$$ P = V I = V 2 \pi BW U_T C $$

Here, $U_T$ is the thermal voltage which is equal to 26mV at room temperature. From equations 5 and 6 it is clear that in MOS transistors the power is proportional to the square of the bandwidth and the sensor capacitance, whereas in bipolar transistors, the power is linearly proportional to both bandwidth and sensor capacitance. This difference in power consumption vs. sensor capacitance between bipolar and MOS implementations for a signal frequency of 1MHz is shown in Figure 7. From Figure 7 we see that MOS transistors behave similar to bipolar transistors in weak inversion but consume significantly more power in strong inversion for the same performance.

Next, let us consider the design tradeoffs in connection with device noise. The power spectral density for the wide band gate referred noise voltage for MOS transistors is given by equation 7, where K is the Boltzmann’s constant and T is the temperature.

$$ \frac{V^{2}_{n_{MOS}}}{V^{2}_{n_{Bipolar}}} \approx \frac{1}{4} \frac{2m_{Bipolar}}{m_{MOS}} $$

It is clear from equation 9 that the transconductance of the MOS devices (M1 and M2) should not be made significantly smaller than the transconductances of the bipolar transistors (B1 and B2). We select a transconductance ratio of 10, i.e., the MOS transconductances are 10X smaller which results in a 10dB loss in SNR. However, the current ratios are 1 to 4, i.e., MOS power is one fourth the bipolar power. This still results in a 10X savings in power. We are able to exploit the particulars of our design requirements for this new design. For our design, the sensor capacitance is 100pF due to other processing constraints and the bandwidth is 1MHz. Our SNR requirement of 60dB results in a minimum capacitor size of about 4.45pF. Clearly, this is much larger than is required from a noise perspective. We are therefore, able to trade off slightly increased noise for lower power with our new circuit.
response of the system. The plot on top shows the voltage regulator output. As expected, the voltage is steady at 5V, with less than a 1mV ripple. The plot in the middle shows the transient output of the sensed and amplified signal from the output of the voltage amplifier. As seen this has a peak-to-peak voltage of about 1V. The last plot is the final output from the external amplifier. As expected, this signal has a peak-to-peak voltage of 1V and a phase shift of 180 degrees from the amplified sensor signal. This change in phase is due to the inverting nature of the external amplifier.

Finally, the layout for the complete system is shown in Figure 10. As can be seen from the layout, most of the area in the chip is occupied by the well resistors and the capacitance. The complete design was sent to be fabricated to MOSIS on the AMI L.2u CMOS with bipolar option. The measurement results will be presented at the conference.

4. CONCLUSIONS

In this paper we presented a design for a two-wire telemetry and signal conditioning circuit for piezoelectric sensor. The telemetry system uses a on-chip voltage regulator as part of the signal-vss-supply filter. We also introduced a new shielded-base bipolar op-amp design that exploits the properties of both MOS and bipolar transistors. The new design results in 10X reduction in power for a 10dB reduction in signal-to-noise ratio.

5. REFERENCES


