A High Speed Differential to Single-Ended Amplifier for Instrumentation Applications

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Abstract

This paper describes a 1GHz differential to single-ended amplifier for instrumentation. The unity gain amplifier can directly drive a 50Ω load with a common-mode voltage centered at ground and can accept up to a 1 V_p-p input signal. The measured noise floor is below 20nV/√Hz for most of the bandwidth and the common-mode rejection is 20dB at 1GHz.

1. Introduction

Many integrated high frequency designs are implemented as fully differential circuits. However, most test equipment (such as spectrum and network analyzers) has connections for single-ended inputs only. This problem is usually solved by using differential to single-ended probes. This paper describes a 1GHz differential to single-ended integrated amplifier that can be used in many applications to test fully differential systems.

This design targets the disk drive industry; however, it should find applications in many other areas. The disk drive industry grows at a staggering pace with data rates fast approaching 500Mbits/s and beyond [1][2]. As data rates increase, so do the requirements for bandwidth on disk drive preamplifiers. Disk drive preamplifiers currently have bandwidths up to 300MHz [2]. These preamplifiers are connected between the read/write heads and the channel. Current state of the art disk drives use magnetoresistive (MR) sensors that require a current or voltage bias. Resistance values for these MR elements typically range from 25 to 75 ohms with a resulting noise density (4KTR) of about 1nV/√Hz. The input referred noise requirement for the preamplifier is usually slightly less than 1nV/√Hz so the signal-to-noise ratio will not be degraded, which can cause an increase in bit error rates. As typical gains of preamplifiers range from 100 to 250, the output referred noise can range from 100-300nV/√Hz.

MR preamplifiers currently have bandpass transfer functions. The high pass corner is usually designed to range from a few hundred kHz to a few MHz to block the bias on the magnetoresistive sensor, yet be low enough to read low frequency servo data. The low pass corner is designed to be high enough so that the high frequency data is not degraded. Disk drive preamplifiers are available as both single-ended and differential at the input side (MR side) and are typically differential on the output. Preamplifier input and output impedances also tend to vary. To make bandwidth measurements, a probe would need to be placed across the magnetoresistive element at the signal input which would tolerate the DC offset on the sensor. Another probe would then be placed at the output, which has a different DC common-mode voltage and the two probes would be normalized before taking the measurement. A differential high impedance amplifier is needed in testing these preamplifiers for gain, bandwidth, and noise. The bandwidth of the amplifier needs to exceed the bandwidth of the preamplifier if the bandwidth measurement is to be accurate. The noise of the amplifier also needs to be small compared to the output noise of the preamplifier.

Most test equipment, such as network analyzers and spectrum analyzers, have specifications on the level of DC offset that can be tolerated for proper function. Some devices cannot tolerate a DC offset. This circuit has been designed with a 50Ω output impedance and a DC offset centered at ground, allowing it to be directly connected to test equipment. The amplifier can be used in test setups for detailed characterization or in applications in which only an integrated circuit can be used.

The amplifier has unity gain and can accommodate a 1 V_p-p input signal. The measured noise floor is less than 20nV/√Hz for most of the bandwidth. The CMRR is below 40dB at low frequencies and 15-20dB at 1GHz. The circuit was fabricated on a BICMOS process with ft=7GHz for a typical device and ft=13GHz for a selectively implanted device that would have a lower breakdown and higher beta. Design and layout considerations, as well as results are discussed.

2. Circuit Design

2.1 Circuit Architecture

The circuit topology was derived from high frequency design concepts and from many of the constraints mentioned in the introduction [3]. Fig. 1 shows a schematic of the amplifier. The inputs contain DC blocking capacitors, C1 and C2, which are used to block the large DC offset on the MR element. The capacitors are followed by emitter followers, Q1 and Q3. The signal then goes to a gain stage, in which the differential to single-ended conversion is done. This stage is composed of transistors Q7 and Q11, and resistors R8, R6, and R9. Emitter followers Q14 and Q16 cascade into C4, which is another DC blocking capacitor. This is used in connection with a gm-C feedback loop to keep the output voltage at ground. The signal then passes through Q18, Q20, and Q22 and has a 50Ω resistance to the output. The 50Ω resistance, R18, isolates the emitter follower from pad and bond wire parasitics and reduces signal peaking.
Dual +5 and -5 Volt supplies were selected for the amplifier due to headroom constraints and the need to accommodate an output common mode voltage centered at ground. Additionally, many differential preamplifiers also use ±5Volt supplies.

2.2 Input Capacitance

The input capacitance was designed to be less than 2pF to attain the required bandwidth. Emitter followers were used on the input for this reason. The emitter followers effectively isolate the input capacitance of the differential pair (Q7 and Q11 of Fig. 1). Cπ, the parasitic base-emitter capacitance of the input devices Q1 and Q3, is essentially reduced by the transconductance multiplied by the input resistance of the differential pair [4]. The input capacitance is determined by the parasitic capacitance to the substrate on the input capacitors, the ESD devices, pad capacitance, and Cπ of the emitter followers Q1 and Q3. Additionally, emitter followers essentially beta multiply the input impedance of the differential pair Q7 and Q11 which makes the input resistance very high. This then allows for a resistor to be used to set a pole, which contributes to the overall high-pass corner of the amplifier. This pole is set by the input DC blocking capacitor C1 and resistor R2 biasing the emitter follower. The capacitor had to be minimized to keep the parasitic capacitance small. High beta devices were used for both the input emitter follower devices and the input differential pair devices to make the impedance looking into Q1 and Q3 large.

2.3 Gain

To obtain an overall unity gain the initial gain stage was set to have a gain of four. This compensates for the loss of gain during the single-ended conversion (one half) and the loss across the output termination resistor (one half), assuming a load resistor of 50 ohms. The overall gain was made to be a function of resistor ratios only. The tail current for the gain stage is proportional to absolute temperature (PTAT). The circuit that makes up the core PTAT bias is shown in Fig. 2 and consists of Q4, Q9, R2, and R7. The same resistor type used in the PTAT core is used for emitter degeneration (R8 of Fig. 1) and the collector resistors R6 and R9, also shown in Fig. 1. Emitter degeneration was used to accommodate the dynamic range of the signal input. Typical signal levels from the output of the preamplifier will be in the hundreds of millivolts. The amplifier was designed for a 1 Volt peak-to-peak input signal. Gain variation can mainly be attributed to the output resistor variation with process.

2.4 Bandwidth

The bandwidth of the amplifier is designed to be over 1GHz with a bandpass response. Multiple emitter-follower stages were used to provide a strong impedance mismatch and allow the circuit to have a high cutoff frequency [3]. The low-pass corner was set by the combination of the gain setting resistors (R8 and R9 of Fig. 1) and the parasitic capacitances at their terminals. The high-pass corner is set by the RC pole at the input and the feedback loop which has a gm-C pole. The gm-C is connected to a MOS device that sets another pole with the 2nd DC blocking capacitor C4 and resistor R14, which is used to bias the emitter follower. The feedback loop introduces two zeros and two poles. Using circuit analysis on the feedback loop portion of the amplifier, and assuming no loss in the emitter followers and a 50Ω load, the overall gain is given by (1).

\[
\frac{V_{out}}{V_{in}} = \frac{1}{2} \left( \frac{s^2}{s^2 + s \cdot \frac{1}{C4 \cdot R14}} + \frac{GM \cdot GM_{M1}}{2 \cdot C5 \cdot C4} \right)
\]

Which puts two zeros at zero and two poles at the following locations (2).

\[
\omega_{1,2} = \frac{-1}{2 \cdot C4 \cdot R14} \pm \frac{\sqrt{C5 - 2 \cdot GM \cdot GM_{M1} \cdot C4 \cdot R14^2}}{2 \cdot C4 \cdot R14 \cdot \sqrt{C5}}
\]
Substituting the following values from the design: $R_{14} = 130\,\text{k}\Omega$, $C_4 = 25\,\text{pF}$, $C_5 = 275\,\text{pF}$, $G_{M1} = 70\,\mu\text{S}$, and $G_M = 0.8\,\mu\text{S}$, gives poles at $2\,\text{kHz}$ and $45\,\text{kHz}$. The high-pass RC pole at the front-end of the amplifier is calculated to be at $35\,\text{kHz}$ given that $C_1$ is $60\,\text{pF}$ and $R_2$ is $75\,\text{k}\Omega$. That gives an overall high-pass corner of $57\,\text{kHz}$.

### 2.5 Noise

Typically in a differential circuit, the noise from the current source will be common-mode and will produce no differential output [5]. In this design, since the output is taken single-ended, most of the noise comes from the current source, especially at low frequencies. For example, the PTAT current source that biases the bases of all the current mirrors was designed with an RC filter to attenuate low frequency noise. The filter was set for a frequency of $35\,\text{kHz}$ using $R_{10}$ of Fig. 2 at $115\,\text{k}\Omega$ and $C_2$ at $40\,\text{pF}$. Layout techniques were used throughout the design to incorporate low-noise transistor layouts (essentially devices that had multiple base stripes for low base noise). The noise decreases at higher frequencies due to the RC filter on the bias and the feedback loop noise being shunted.

### 2.6 Common-Mode Rejection

Common-mode rejection is greater than $40\,\text{dB}$ at low frequencies. The differential pair input devices were minimized to improve the common-mode rejection. This device was also minimized to prevent possible oscillation by having a large capacitive load on the input emitter followers [6]. A simplified circuit using Q7, Q6, and R6 of Fig. 1 was used to calculate the common-mode gain of the circuit. The output resistance of Q8 was modeled. The low-frequency common-mode gain is given by (3).

$$A_{CM} = \frac{g_{m7} \cdot R_6}{1 + g_{m7} \cdot r_{o8} + \frac{r_{o8}}{\beta_{Q7}}}$$

This results in CMR of $-46\,\text{dB}$ for the following parameters $g_{m7} = 100\,\mu\text{S}$, $R_6 = 500\,\Omega$, $r_{o8} = 100\,\Omega$, and $\beta_{Q7} = 100$. The common-mode gain than has a zero at the following location (4).

$$\omega_{zero} = \frac{g_{m7}}{2 \cdot C_{\pi Q7}} \left[ 1 + \frac{4 \cdot C_{\mu Q7}}{C_{\mu Q7} \cdot r_{o8} \cdot g_{m7}} \right]^{-\frac{1}{2}}$$

This zero occurs at $8\,\text{MHz}$ using $C_{\mu} = 2\,\text{pF}$ and $C_{\pi} = 2\,\text{pF}$. The gain increases until around $1.5\,\text{GHz}$ where there is a pole due to the gain resistor and base-collector capacitance of the cascode device. The location of the zero which starts the gain increasing, is mainly determined by $C_{\mu}$. For this reason, the input device was made as small as possible.

### 2.7 Layout

The layout was carefully designed for symmetry. Even though the circuit only requires a single-ended output, the whole differential path was mirrored. Inputs come in on one side of the die and leave from the other to minimize any possible feedback or crosstalk. Traces on all emitter followers were minimized to prevent capacitive loading and prevent peaking in the amplifier response [7]. The microphotograph is shown in Fig. 3.

3. Results

The bandwidth of the amplifier was measured with a Hewlett Packard 8753D 30kHz-3GHz network analyzer as shown in Fig. 4. One of the inputs was connected to ground and the other input had a $50\,\Omega$ termination resistor to ground to which the signal was connected. The amplifier was effectively being driven single-ended. The network analyzer signal was normalized, by connecting the cables from input and output together. Some of the test board and package parasitics (bond-wires) are not taken into account in the normalization. The bandwidth is not perfectly flat for this reason and there is some peaking beyond $1\,\text{GHz}$. This can be reduced by using bump, double bond wires, or by adding another pole to the amplifier. The output was taken directly from the amplifier to the network analyzer. Figure 4 shows the high pass corner at $55\,\text{kHz}$, and the bandwidth extending up to $1\,\text{GHz}$. Common-mode rejection, shown in Fig. 5, was measured to be greater than $40\,\text{dB}$ at low frequencies and $15-20\,\text{dB}$ at $1\,\text{GHz}$.
Noise measurements were made using a Hewlett Packard 8560E spectrum analyzer and are shown in Fig. 6. The amplifier noise was measured by shorting the inputs together and connecting the output to a spectrum analyzer. The results then had the noise floor for the spectrum analyzer (measured separately) removed. The overall noise was less than 20nV/√Hz, which when compared to 100-300nV/√Hz at the preamplifier output, is sufficiently low as to not impact the measurement results.

![Figure 4. Amplifier Frequency Response](image)

![Figure 5. Common-Mode Rejection](image)

![Figure 6. Noise Plot](image)

### 4. Conclusion

A 1GHz differential to single ended output amplifier has been realized. The IC can directly drive a 50Ω load and has an output common mode voltage centered at ground. The amplifier is unity gain and has a dynamic range that can accommodate a 1 V P-P input signal. The noise is less than 20nV/√Hz with common-mode rejection of 20dB at 1GHz.

### 5. References


