A 455-Mb/s MR Preamplifier Design in a 0.8-μm CMOS Process

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Abstract—In this paper, we present a CMOS preamplifier for use with magnetoresistive (MR) read elements in disk drives. The performance of the CMOS design is competitive with the more expensive current generation of BiCMOS MR preamplifiers. The measured gain for the preamplifier is 43 dB and the measured 3-dB bandwidth is greater than 273 MHz corresponding to a 455-Mb/s data rate. Likewise, the measured input-referred voltage noise is less than 0.57 nV/√Hz, and measured input-referred current noise is less than 10.54 pA/√Hz at an MR bias current of 10 mA. The preamplifier has been implemented in a 0.8-μm 5-V CMOS process and occupies a die area of 1.78 × 1.78 mm². In this paper, we introduce a new scheme to reduce current noise below that contributed by a single MOS device. This technique has the potential for even more impact for future submicron processes. We also showed that voltage amplifiers offer lower noise than transimpedance amplifiers for similar gain and bandwidth constraints.

Index Terms—Amplifier noise, disk drives, HF amplifiers, MOSFET amplifiers.

I. INTRODUCTION

The disk drive magnetoresistive (MR) preamplifier market has been dominated by BiCMOS preamplifiers. In addition, the preamplifier market has become more competitive in recent years as pricing pressures increase. A CMOS-only MR preamplifier is attractive due to the lower fabrication cost associated with the simpler process. A few CMOS MR preamplifiers have been described in the literature [1]–[3], but they do not achieve current performance of commercial parts in terms of both bandwidth and noise. This paper describes the design of a CMOS-only MR preamplifier that meets both the noise and bandwidth specifications and is competitive with the more expensive BiCMOS MR preamplifiers used in current generation disk drives. We achieved our results and presented them in [5], [6]. Subsequent to that time, Lam and Cheng [4] achieved similar performance.

A. System Requirements

In a typical disk drive system, there are several disk surfaces, each of which requires a MR read element to read data from that disk. Therefore, the preamplifier must have an input for each MR element. In addition, MR read elements need to be biased with optimal dc bias currents in order to maximize their output signals and linearize their response. Out preamplifier circuit is designed to bias and sense input signals from four separate MR elements. This requires four sections of the preamplifier front-end circuitry, one for each MR head, which are multiplexed together into a common back-end amplification stage. Since MR heads can have differing output characteristics due to normal process variations, the MR bias current provided by the preamplifier must be adjustable. For this purpose, our preamplifier circuit contains a 5-b digital-to-analog converter (DAC) with a programmable current range of 2–10 mA.

Another constraint with MR read elements is that the common-mode voltage of the head needs to be kept near ground to avoid arcing to the disk. This was one of the factors in choosing a single-ended input architecture, where one side of the MR head is tied directly to ground, thus requiring no extra effort to achieve the desired common-mode voltage. If a differential input architecture were chosen, a costly negative power supply would be needed as well as a common-mode feedback loop.

The electrical signal produced by the MR head element is on the order of a few hundred microvolts. Since the signal level is quite low, the preamplifier is required to provide high-gain low-noise amplification before the data can undergo subsequent signal processing by the channel electronics. Typical preamplifier gains range from 100 to 300 V/V [7]. The CMOS preamplifier was designed for a nominal gain of 200 V/V. Disk drive preamplifiers have rigorous noise requirements as noise can degrade bit-error-rate performance. The total preamplifier noise includes both the noise from the amplifier (voltage noise) as well as the noise from the DAC that generates the dc current for the MR element (current noise). The current noise is converted to voltage noise at the preamplifier input by multiplying it with the resistance of the MR element, \( R_{\text{MR}} \). It is then added in an RMS fashion to the voltage noise to give the total preamplifier noise. Since this total noise depends on the value of \( R_{\text{MR}} \), which tends to vary, the preamplifier noise is often specified as separate voltage and current noise. Typical input-referred noise specs for state-of-the-art preamplifiers are 0.6 nV/√Hz voltage noise and 10 pA/√Hz current noise [7]. The CMOS preamplifier presented in this paper has been designed to meet both of these noise requirements.

The required frequency response of the preamplifier is that of a bandpass with a high-pass corner frequency ranging from hundreds of kilohertz to a few megahertz and a low-pass corner frequency high enough to meet the targeted data rate. With current data rates nearing 500 Mb/s, the preamplifier bandwidth requirement set by this low-pass corner is around 300 MHz, which was the design goal of this preamplifier [7].
TABLE I
SUMMARY OF SYSTEM REQUIREMENTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>200 VV or 46 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>&gt; 300 MHz</td>
</tr>
<tr>
<td>Input-referred Voltage Noise</td>
<td>&lt; 0.6 nV/√Hz</td>
</tr>
<tr>
<td>Input-referred Current Noise</td>
<td>&lt; 10 pA/√Hz</td>
</tr>
<tr>
<td>MR Bias Current (I_{mr})</td>
<td>2-10 mA</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>5V (+10%)</td>
</tr>
<tr>
<td>MR Resistance (R_{mr})</td>
<td>(40 ± 10)Ω</td>
</tr>
<tr>
<td>MR Interconnect Inductance (L_{mr})</td>
<td>(30 ± 10) nH</td>
</tr>
<tr>
<td>Number of MR Inputs</td>
<td>4</td>
</tr>
<tr>
<td>Power Dissipation (I_{mr} = 10 mA)</td>
<td>350 mW</td>
</tr>
</tbody>
</table>

Fig. 1. Simplified top-level diagram.

The high-pass corner blocks the dc bias on the MR element and filters the low frequency noise of the MR bias current. Its frequency is set to be low enough such that the low frequency servo data can be read. The high-pass corner is set by a feedback transconductance amplifier along with on-chip ac coupling. No external capacitors are needed with this preamplifier design.

Other system requirements include a single 5-V power supply with a ±10% tolerance, a 40-Ω \( R_{m} \) with a ±10-Ω variance, and a 30-nH parasitic interconnect inductance with a ±10-nH variance. The above-mentioned system requirements are summarized in Table I.

II. CIRCUIT ARCHITECTURE

A. Architecture Overview

A simplified block diagram for the overall circuit is shown in Fig. 1. There are four parallel sections of the front-end circuit, or head cells, corresponding to the four MR element inputs. The rest of the circuit is common and is comprised of an \( I_{mr} \) DAC, first and second amplification stages, and a \( gm \) feedback stage. A simplified circuit schematic for a single path of the preamplifier circuit is shown in Fig. 2. Here, only one MR element is biased and sensed. The other three MR elements and their associated head cells are off and are not shown. The components found in each head cell are M1, C1, and M6. We note in Fig. 2 that the current from the \( I_{mr} \) DAC flows through the selection/cascode device M6 to bias the selected external MR element. The signal from the MR element is ac-coupled through C1 onto the gate of the common-source input device M1. The signal is converted to a current by the input device M1 and enters the first cascode device M2. Since each MR head cell has an input device M1, the drains of four input devices are connected together at the source of M2, multiplexing into the common first-stage gain cell. Following M2, the signal passes through the second cascode device M3 and is converted back to a voltage by the load resistor R1 at the first-stage output. Since the preamplifier input is single-ended and the preamplifier output needs to be differential, single-ended-to-differential conversion is done at the first-stage output VRP-VRN by the \( gm \) feedback loop. Performing the conversion here allows the use of a conventional differential amplifier for the second stage. Details of this conventional differential amplifier are not presented here.

The single-ended input architecture is attractive for MR preamplifiers for several reasons. As already mentioned, the common-mode voltage of the MR element is near ground as required without any further work. A differential input architecture would require a common-mode feedback loop as well as a negative supply, which increases power dissipation and system cost. Since the single-ended input architecture has only one input device as opposed to two with differential input architectures, area and power are reduced. Furthermore, with fewer noise-contributing devices, the equivalent input noise is also reduced. One disadvantage of the single-ended input architecture is the lack of common-mode rejection. However, differential input architectures also have CMR problems, although to a lesser extent, because it is difficult to achieve good CMR at high frequencies. In fact, most differential input architectures exhibit greater than unity common-mode signal gain above 100–200 MHz. For these and cost reasons, single-ended input designs are preferred for data rates less than 500–600 MHz, but fully differential input designs may still provide some limited benefits for higher data rates.

The architecture of this preamplifier is also referred to as a voltage-sense architecture because the signal voltage is sensed by the high-impedance gate of the input device M1. An alternative design is a current-sense architecture, where the non-ground side of the MR element is tied to the low-impedance source of a common-gate input device and the signal current is sensed. One advantage of the current-sense architecture is lower power since the MR element bias current and input device current are shared. Another advantage with the current sense approach is the suppression of resonant peaking at the preamplifier input, which will be discussed later. However, more importantly, the current-sense architecture has a fundamental disadvantage in terms of the first-stage gain–bandwidth tradeoff. For the same first-stage gain-setting resistor, the current-sense architecture will have a lower gain value than the voltage-sense architecture because the gain is inversely proportional to the impedance seen in the source of the input device M1 and this impedance is larger for a current sense (\( R_{m} \)) than for a voltage sense (1/\( m \)) circuit. To achieve the same first-stage gain, the gain-setting resistor for the current-sense architecture needs to be much larger than for the voltage-sense architecture. This reduces the preamplifier bandwidth since the dominant pole is the \( RC \) pole at the first-stage output. As a result,
either the bandwidth or the first-stage gain of a current-sense architecture can be made equal to that of a voltage-sense approach, but both cannot be done simultaneously. This is important because a large first-stage gain is essential to achieve low equivalent input noise in the preamplifier. With a large first-stage gain, the second-stage devices become negligible noise contributors when referred back to the preamplifier input. Therefore, to achieve the best overall gain-bandwidth-noise solution, the voltage-sense architecture was chosen for this design.

Previous voltage-sense amplifiers have used a transimpedance amplifier topology [2], [4]. However, we use a voltage amplifier due to its improved noise performance. This is illustrated with the help of Fig. 3. The left-hand side of this figure shows the traditional transimpedance amplifier used in [2], [4]. The transimpedance amplifier uses a feedback resistance \( R_f \) from the drain node to the gate node. While the right-hand side of the this figure shows a simple voltage amplifier that uses a load resistance \( R_L \) from the drain node to an ac ground. For our next discussion, we assume that the output conductance is small and the gain is primarily set by the product of the transconductance and load resistances. The voltage noise contribution of the feedback/load resistors \( R_f \) and \( R_L \) at the output are given by \( 4kT R_f \) and \( 4kT R_L \) respectively, i.e., the noise contribution is the same provided that the resistor values are the same. The input–output gain for the transresistance amplifier is given by

\[
\frac{V_o}{V_{rmp}} = -g_\text{m1} R_f \left( 1 - \frac{1}{g_\text{m1} R_f} \right) \tag{1}
\]

while the gain for the voltage amplifier is given by \( g_\text{m2} R_L \).

If we assume that the size, power level, and resultant noise contributions are the same for transistors \( M_1 \) and \( M_2 \), then the necessary value for \( R_f \) for the two gains to be the same is given by

\[
R_f = R_L \left[ 1 + \frac{1}{A_V} + g_\text{m} R_{\text{mnr}} \right] \tag{2}
\]

If we assume that the first-stage gain is larger than ten, the value of \( 1/A_V \) is negligible. However, as we will discuss in Section III, to keep the noise contribution of the input transistor lower than the noise contribution from the MR sensor \( g_\text{m} R_{\text{mnr}} \).
is usually much larger than one. Therefore, to obtain the same gain, the value of the feedback resistance in the transresistance amplifier has to be much larger than the value of the load resistance in the voltage amplifier. Using our earlier discussion, that the load/feedback resistance contributed noise power spectral density at the output of the first gain stage is given by $4kTR_n$, the noise level of the transresistance-based voltage sense technique is inherently higher than that of a voltage-amplifier-based voltage sense technique for MR preamplifiers. So, though the noise from the MR element, the input DAC, and the input transistor still dominate, we have chosen to use the voltage-amplifier-based voltage sense technique for our design because of the extremely stringent noise requirements. Similar conclusions for low-noise amplifiers in other applications have been reached by other authors as well [9]. However, this paper provides the first analytic justification for this conclusion.

The feedback implemented by the transconductance amplifier or $gm$ stage in Fig. 2 performs several functions [10]. As previously mentioned, the $gm$ feedback performs the single-ended-to-differential conversion at the first-stage output. In addition, it sets the current through the gain-setting resistor $R_1$ and second cascode device $M3$ by forcing a voltage across $R_1$. This voltage is set by a reference current dropped across $R_2$, which is scaled and matched to $R1$. The amount of current through $R1$ and $M3$ is limited by the headroom. As will be discussed shortly, additional current is then summed with this current to bias $M1$ and $M2$. The $gm$ feedback also forces $VRP$ and $VRN$ to the same dc potential, which minimizes the dc offset of the first stage and ultimately the preamplifier output. Finally, the $gm$ feedback along with the first-stage gain and on-chip ac-coupling capacitor $C1$ determine the location of the high-pass corner frequency. Referring to the simplified block diagram shown in Fig. 4, the transfer function for the preamplifier can be shown to be given by

$$\frac{V_o}{V_i} = \frac{Av_1 Av_2}{1 + \frac{Av_1 gm}{sC_1}}.$$  

This transfer function has a highpass characteristic with a corner frequency given by

$$f_{-3dB} = \frac{Av_1 gm}{2\pi C_1}.$$ 

The low-pass corner of the transfer function is determined by the high-frequency poles of the amplifier, primarily in the first stage. Since $C1$ is on chip and in every head cell, it is preferable to keep $C1$ small in order to minimize chip area. In addition, the parasitic capacitance of $C1$ contributes to the preamplifier input capacitance, which reduces bandwidth. By setting the on-chip $C1$ to be equal to 100 pF, the high-pass corner frequency for this reader was set at a nominal value of 1.75 MHz. Also, because the $gm$ feedback stage is common to all heads, a passgate is used to connect the $gm$ stage to the selected head and isolate it from the unselected heads.

B. Key Design Issues and Tradeoffs

There are several tradeoffs involved with the input device $M1$. Most importantly, its transconductance or $gm$ needs to be maximized in order to achieve large first-stage gain and low noise. The first-stage gain, the importance of which has already been described, is directly dependent upon the $gm$ of the input device $M1$ by

$$Av_1 = K gm_1 R_1$$

where $K$ is an attenuation factor due to parasitics and is discussed in the next paragraph.

The input device $M1$ is the largest on-chip noise contributor, with only the external MR element contributing more noise. It is therefore essential to minimize its noise. As will be shown in the next section, this can also be accomplished by maximizing the input device $gm$. To achieve a large $gm$ for $M1$, its $W/L$ and drain current $I_{ds}$ can be increased. Both of these were maximized to their practical limit. The upper limit for the $W/L$ of $M1$ is due to power dissipation. The gate capacitance is the main contributor to the preamplifier input capacitance, which reduces bandwidth through an $RC$ pole at the input as well as resonance with the parasitic interconnect inductance $L_{PIR}$. Furthermore, the input device gate capacitance, along with the ac coupling capacitor $C1$, causes capacitive attenuation which reduces the gain. This is one of the main contributors to the $K$ factor in (5) and is the primary factor in how small $C1$ could be sized. The drain capacitance of the input device also affects bandwidth, as all four head cells have their $M1$ drains connected at the source of $M2$. This is a large capacitive load for the first cascode device source to drive. Therefore, the $1/gm$ of $M2$ also needs to be small to minimize the effect of this $RC$ pole on the total preamplifier bandwidth. The upper limit for the input device drain current $I_{ds}$ is determined by power

![Fig. 4. Simplified reader block diagram.](image-url)
dissipation constraints. Its $g_m$ can be driven arbitrarily low by continuing to increase the drain current. Thus, there is a performance versus power tradeoff. Given these tradeoffs and the values of $R_{int}$, $L_{int}$, desired power dissipation, and number of MR heads for this design, a $W/L$ of 2000/0.8 and $I_{ds}$ of 24 mA were chosen for the input device M1.

In addition to bandwidth concerns, the first cascode device M2 also needs a large $g_m$ to prevent signal attenuation from the extremely low output impedance of M1, which is due to the large drain current and minimum gate length. Signal attenuation is undesired because it reduces the first-stage gain, which increases the input-referred noise. A high $g_m$ for M2 was achieved by setting $W/L = 2500/0.8$ and using the same 24-mA drain current from the input device M1. As described earlier, the $g_m$ feedback sets the current through R1 and M3. The amount of this current is limited to about 6 mA as determined by the maximum voltage drop across R1 that still keeps M3 biased in the saturation region. The remaining 18 mA required to bias M1 and M2 are provided by a current source injected between M2 and M3. The physically large current source was added here, where its parasitic capacitance can be driven by the source of M3, instead of at the gain-setting node where it would severely degrade the bandwidth. This also provides more headroom for the current source.

The second cascode device M3 is needed to avoid the large amount of signal attenuation that would otherwise occur due to the low output impedance of M2. Even though M2 is a cascode device, it still has a relatively low output impedance compared to the 390-$\Omega$ load resistor R1 due to M2’s large drain current and minimum gate length along with M1’s very low output impedance. Choosing the value of R1 involved trading gain versus bandwidth. To maximize the first-stage gain, R1 needs to be made large. However, doing so reduces the frequency of the $1/RC$ pole at this node, which is the dominant pole. In order to maintain high bandwidth, the capacitive loading on the gain-setting resistor R1 is minimized by sizing all devices connected to that node as small as possible, while still considering the other design constraints.

Although measures have been taken to reduce the signal attenuation in the first stage, there is still a significant amount that cannot be neglected due to the small channel lengths and large drain–source currents involved. For example, even in our optimized design, there is a $-1.62$-dB signal attenuation which directly adds to the noise of the system. Fig. 5 shows a simplified first stage with parasitic components, where the gates of M2–M6 represent ac grounds. There are two parts to the overall signal attenuation, front-end attenuation and signal-path attenuation. The overall attenuation factor $K$ [also in (5)] is shown in (6), where $K_{FE}$ represents front-end attenuation that occurs before the signal from the MR element even reaches the gate of the input device M1. Unlike the front-end attenuation, the signal-path attenuation is only a function of parasitic small-signal output impedances of the transistors as it is dc coupled. Parasitic capacitances only limit the bandwidth.

$$K = K_{FE} \left( \frac{Z_2}{g_{m2eq}} \right) \left( \frac{Z_3}{g_{m3eq}} \right) \left( \frac{Z_L}{R_1} \right). \quad (6)$$

The midband front-end attenuation, which consists of both capacitive and resistive components, can be shown to be given by

$$K_{FE} = \left( \frac{C_1}{C_1 + C_{par1b}} \right) \left( \frac{R_{fb}}{R_{fb} + R_{int}} \right) \quad (7)$$

where $R_{fb}$ is the effective impedance forced by the $g_m$ feedback loop.

From (4), this effective impedance is given by

$$R_{fb} = \frac{1}{Av_1 g_m}. \quad (8)$$

The amount of capacitive front-end attenuation is dependent on the size of both $C_{par1b}$ and C1. The parasitic capacitance $C_{par1b}$ is mainly due to the gate capacitance of the input device M1, and was a factor in how large M1 could be made. Equation (7) also constrained how small the on-chip ac coupling capacitor C1 was made. For example, without this constraint, C1 could have been made smaller, along with the feedback $g_m$ to keep the same highpass corner frequency, but was kept at 100 pF to reduce capacitive attenuation $= 0.83$.

The Z terms in the numerator of (6) represent the node impedances shown in Fig. 5, and the $1/Gm_{eq}$ terms in the denominator represent the impedance seen looking into the source of the respective cascode device. Ideally, $Z_2 = 1/Gm_{2eq} = 1/gm_2$, $Z_3 = 1/Gm_{3eq} = 1/gm_3$, and $Z_L = R_1$, which yields no attenuation from the gate of M1 to R1. In reality, the large drain currents and minimum gate lengths used in the first stage cause low output impedance and therefore attenuation. The impedance at the node between M1 and M2 is

$$Z_2 = \frac{1}{Gm_{2eq}} |r_ds_1|. \quad (9)$$

The signal is attenuated because the output impedance of M1 is small enough to shunt some of the small signal current away.
from the low source impedance of M2. As already mentioned, this is one reason that the $1/gm$ of M2 was minimized. However, the impedance seen looking into the source of a cascode device is not simply $1/gm$ (as normally assumed) due to the finite output impedance of that device and also the nonzero load resistance $R_L$ seen by its drain. This impedance, defined here as $1/Gm_{eq}$, needs to be found in order to correctly determine the amount of attenuation due to the output impedance of the device below. Using the low-frequency small-signal model, the impedance seen looking into the source of a MOS cascode device can be shown to be given by

$$\frac{1}{Gm_{eq}} = \frac{1}{gm} \left[ \frac{1 + \frac{R_L}{rds} \frac{1}{gm \cdot rds}}{1 + \frac{1}{gm \cdot rds}} \right]$$

(10)

where the gate is assumed to be ac ground, and $gm$ and $rds$ are for the cascode device whose source impedance is being evaluated.

The validity of (10) can be verified by individually removing the parasitics. If $rds$ is set to be equal to $\infty$, then $1/Gm_{eq} = 1/gm$. In a similar manner, if $R_L$ is set to zero, then $1/Gm_{eq} = (1/gm)[rds]$. For M2, $R_L = (1/Gm_{eq})[rds]$, and for M3, $R_L = R_L$. The impedance at the node between M2 and M3 is given by

$$Z_3 = \frac{1}{Gm_{eq} \cdot rds}$$

(11)

and the impedance at the node between M3 and $R_1$ is given by

$$Z_L = R_L \cdot rds$$

(12)

Nominal simulation results show that the overall attenuation, given in the order shown in (6), is $(0.92)(0.935)(0.975)(0.99)$ = 0.85, i.e., $-1.62$ dB. The first term, $K_{FE}$, has equal contributions of 0.96 from the capacitive and resistive components. The largest attenuation factor of 0.935 is due to the low output impedance of the input device M1 affecting $1/Gm_{2eq}$. The large output impedance of the second cascode device M3 causes only a 1% attenuation on the load resistor $R_1$. If a second cascode were not used, the attenuation at that node would have been much larger, about 15%. Despite the attenuation, the overall first-stage gain is still large enough (about 36 V/V) to make the input-referred noise of the second stage negligible.

The large first-stage gain also allows a much smaller gain for the second stage, which creates higher frequency poles that do not degrade the preamplifier bandwidth. Thus, the preamplifier bandwidth can be approximated using only the first-stage poles. Fig. 5 shows that there are four nodes in the first-stage signal path, each contributing an $RC$ pole. The node impedance equations for $Z_2$, $Z_3$, and $Z_L$ are given in (9), (11) and (12), respectively. The input node impedance $Z_{in}$ is equal to $R_{in} || R_{th}$. The total parasitic capacitance for each node shown in Fig. 5 is the sum of all the device parasitic capacitances attached to that node. Using these node impedance and capacitance terms, the overall preamplifier 3-dB bandwidth can be approximated using

$$f_{-3dB} \approx \frac{1}{2\pi \sqrt{\left(\frac{Z_{in} \cdot C_{in}}{2}\right)^2 + \left(\frac{Z_3 \cdot C_3}{2}\right)^2 + \left(\frac{Z_L \cdot C_L}{2}\right)^2}}$$

(13)

The nominal simulated bandwidth exceeds 300 MHz and is shown in Fig. 6.

An additional system level issue that should also be mentioned is peaking in the preamplifier gain response due to series resonance at the preamplifier input. Fig. 6 shows the simulated preamplifier frequency response with and without $L_{mr}$, where $R_{mr} = 40 \Omega$ and $L_{mr} = 30$ nH were used. Notice the high frequency peaking in the case with $L_{mr}$. Fig. 7 shows a model for the preamplifier input circuit. The source $V_s$ represents the signal from the MR element, $C_{in} = C_{var}$, $R_{in} = R_{th}$, and $V_o$ is the signal seen by the preamplifier. As can be seen in Fig. 7, series resonance exists at the preamplifier input due to the MR element parasitic interconnect inductance $L_{mr}$ and the preamplifier input capacitance $C_{in}$. This resonance causes undesired peaking in the transfer function from $V_s$ to $V_o$, which then passes through the preamplifier and is seen at the preamplifier output. The frequency of maximum peaking [11], [12] can be approximated by

$$f_m = \frac{1}{2\pi} \sqrt{\frac{1}{L_{mr} \cdot C_{in}} - \frac{1}{2} \left(\frac{R_{mr}}{L_{mr}}\right)^2}$$

(14)

where the preamplifier input resistance $R_{in}$ is neglected since it is fairly high.
Thus, the smaller $C_{\text{in}}$ is, the higher the peaking frequency. This was a primary reason for keeping the preamplifier input capacitance as small as possible. Ideally, the peaking would occur at a frequency beyond the preamplifier bandwidth and therefore have little effect on signals in the frequencies of interest.

Referring to Fig. 7, the magnitude of the peaking at this frequency is given by [11]

$$V_o\bigg|_{f_m} = \frac{1}{\sqrt{\frac{R_{\text{mr}}^2 C_{\text{in}}}{L_{\text{mr}}} \left(1 - \frac{R_{\text{mr}}^2 C_{\text{in}}}{4L_{\text{mr}}}\right)}}. \quad (15)$$

Qualitatively, the amount of peaking decreases as $R_{\text{mr}}$ increases due to the reduction in the series $Q$. The amount of peaking that can be tolerated by the channel electronics, which performs signal processing after the preamplifier, depends on the frequency and magnitude of the peaking, as well as the ability of the particular channel chip used to deal with such issues as group delay variation.

III. NOISE CONSIDERATIONS

As mentioned in Section II, disk drive preamplifiers have stringent noise requirements. The noise requirements for our CMOS preamplifier are an input-referred voltage noise less than 0.6 nV/\sqrt{Hz} and an input-referred current noise less than 10 pA/\sqrt{Hz}.

It is common practice to refer all the noise to the input terminal. Referring the noise to the input by dividing by the preamplifier gain creates a “bathtub” shape curve since the gain has a passband characteristic. The floor of the bathtub curve extends over most of the preamplifier bandwidth, and is where noise measurements are taken and compared to specifications. Fig. 8 shows the nominal simulated input-referred noise for the total system, $R_{\text{mr}}$, total preamplifier current, and preamplifier voltage noise with $R_{\text{mr}} = 40 \, \Omega$, and $I_{\text{mr}} = 10 \, mA$.

The total system noise, shown as the top curve in Fig. 8, comprises of the RMS sum of the preamplifier and $R_{\text{mr}}$ noise components as shown in

$$v_{\text{inol}} = \sqrt{\frac{v_{\text{rmr}}^2 + v_{\text{vpe}}^2 + v_{\text{cpe}}^2 R_{\text{mr}}^2}{R_{\text{mr}}^2 C_{\text{in}}}} \quad (16)$$

where $v_{\text{rmr}}$ is the MR head thermal noise, $v_{\text{vpe}}$ is the preamplifier voltage noise, and $v_{\text{cpe}}$ is the preamplifier current noise. The dominant individual noise source in the system is the physical resistance of the MR element, whose noise power spectral density is given by $v_{\text{rmr}}^2 = 4kT R_{\text{mr}}$. The second line on Fig. 8 shows $v_{\text{rmr}}$ using a typical value of $R_{\text{mr}} = 40 \, \Omega$.

The preamplifier-only contribution to the noise is given by the last two terms in (16). The simulated value for this result is shown as the third curve in Fig. 8. The preamplifier current noise $v_{\text{cpe}}$ is generated by the $I_{\text{mr}}$ DAC, which creates the MR element bias current. As seen from (16), the current noise is converted to a voltage noise across the head resistance $R_{\text{mr}}$. Since $R_{\text{mr}}$ varies, the voltage and current noise are specified separately. The preamplifier voltage noise is measured by shorting out $R_{\text{mr}}$, which removes the MR element thermal noise and preamplifier current noise from the total system noise. This can be seen by setting $R_{\text{mr}} = 0$ in (16). The bottom curve in Fig. 8 shows the simulated voltage noise. The preamplifier current noise can then be calculated by substituting the known variables into (16).

The dominant noise sources in the preamplifier is the voltage noise of the input device M1 and the current noise of the $I_{\text{mr}}$ DAC. Since M1 is the largest on-chip noise source, every effort was made to minimize its noise. Its gate-referred equivalent input noise power spectral density is given by

$$i_{\text{inol}}^2 = \frac{4kT g_{\text{d}}}{g_{\text{m}}^2} \quad (17)$$
where $\gamma$ is the excess noise factor, $g_{ds}$ is the drain–source conductance for zero $V_{ds}$, and $gm$ is the transistor transconductance. For long channel devices $g_{ds}$ is approximately equal to $gm$ and $\gamma$ is equal to $2/3$. However, for short-channel devices $g_{ds}$ is typically larger than $gm$ and $\gamma$ is larger than $2/3$ ($\gamma \approx 2$ for 0.25-$\mu$m nMOS device [13]).

We have neglected flicker noise because the gate area is large for M1 and because of the 1.75-MHz high-pass corner frequency. As can be seen from (17), the noise of M1 is minimized by maximizing the $gm$. As discussed earlier, this was done by increasing the $W/L$ and drain current to their practical limit while still considering the other design constraints.

Fig. 9 shows a simplified schematic for the MR bias current DAC. The $RC$ filter shown has a corner frequency of less than 10 kHz, effectively blocking any noise from the reference current generator. Again neglecting $1/f$ noise, the power spectral density for the drain–source current noise is given by

$$\overline{I^2} = 4kT \gamma g_{ds} = 4kT \gamma \alpha gm$$  \hspace{1cm} (18)$$

where $\alpha$ is close to one.

Here we note that, unlike the input transistor M1, current noise is minimized by minimizing $gm$. Therefore, the $gm$ for the DAC devices needs to minimized. The traditional method for reducing current noise is to minimize the $gm$ by reducing the $W/L$’s of the MOS devices. This increases the $V_{gs}$ required and is limited by the headroom available. For the same headroom, a lower noise solution is to increase the $W/L$’s and use the headroom for resistor degeneration. This may seem counterintuitive, as it will not only introduce the thermal noise of the degeneration resistor, but also increase the MOS device $gm$ as $W/L$ is increased. However, the input-referred noise is actually reduced by degenerating because the noise transfer function from the $I_{int}$ DAC to the preamplifier input is decreased more than the total DAC device noise is increased. We illustrate this with the help of the circuit in Fig. 10.

The total current noise contributed by the MOS device $M_{dac}$ is given by (19) and that contributed by the resistor is given by (20).

$$\overline{I^2}_{M_{dac}} = 4kT \gamma gm \left( \frac{1}{1 + gmR} \right)^2$$  \hspace{1cm} (19)$$

$$\overline{I^2}_{Rs} = 4kT R \left( \frac{gm R}{1 + gm R} \right)^2$$  \hspace{1cm} (20)$$

Let $I$ be the current through transistor $M_{dac}$ and $\Delta V_{tot}$ be the minimum output voltage. The minimum output voltage across a MOS device in saturation is given by $\Delta V = 2I/gm$ and the voltage drop across the resistor is given by $IR$. If we maintain the same minimum output voltage then the $\Delta V$ for the source degenerated MOS device is given by

$$\Delta V = \Delta V_{tot} - IR_s.$$  \hspace{1cm} (21)$$

Therefore, the necessary $gm$ for the device with nonzero source degeneration resistor is given by

$$gm = \frac{gm_0}{1 - \frac{gm_0}{2}}$$  \hspace{1cm} (22)$$

where $gm_0 = 2I/\Delta V_{tot}$ is the transconductance of the transistor with $R_s$ equal to zero. We see from (21) and (22) that as
Fig. 11. Noise reduction for different values of $\gamma$.

$R_{se}$ increases, the MOS $\Delta V$ decreases and the transconductance increases.\(^2\)

We can now write the total output referred noise for the source degenerated transistor shown in Fig. 10 as

$$
Tn_0^2 = 4kT \gamma g m_0 \left[ \frac{1 - g m_0 R_{se}}{2 (1 + g m_0 R_{se})^2} + \frac{1}{\gamma} \frac{g m_0 R_{se}}{(1 + g m_0 R_{se})^2} \right]
$$

(23)

where the first term inside the square brackets is the noise contribution of the MOS device and the second term is the noise contribution of the resistor.

The maximum possible value for $R_{se}$ given by $R_{se,\text{max}}$ equal to $\Delta V_{\text{sat}}/I$. Substituting this value for $R_{se}$ into the term inside the square bracket in (23) results in $1/(2\gamma)$. So, this is the best-case reduction in output-preferred noise. The magnitude of the term inside the square bracket in (23) has been plotted for two values of $\gamma$, $\gamma = (2/3)$ and $\gamma = 2$, and two signal frequencies, dc and 300 MHz, in Fig. 11. Here, we note that for long-channel devices, $\gamma = (2/3)$, the overall contribution at dc can be reduced to 75% of its original value and for short-channel devices \([13]\), $\gamma = 2$, the contribution can be reduced to 25% of its original value. However, for most practical applications, the maximum value for $R_{se}$ cannot be used because of the reduction in the pole frequency at the source of transistor $M_{\text{hac}}$ in Fig. 10. This is seen for the two traces at 300 MHz. A more realistic value for $R_{se}$ is $R_{se,\text{max}}/2$. But even for this value of $R_{se}$ there is 11% reduction in the noise for $\gamma = (2/3)$ and a 56% reduction for $\gamma = 2$. Therefore, this technique for current noise reduction in current sources is likely to prove even more beneficial for sub-micron technologies.

In many fabrication processes, the resistors have better matching characteristics than MOS devices. So, in addition to noise reduction, source degeneration also results in improved current-mirror matching characteristics \([14]\).

\(^2\)Note that these equations are valid only for strong inversion. When the width of transistor $M_{\text{hac}}$ is made extremely large, the device operates in weak inversion and (21) and (22) are no longer valid.

A number of layout considerations for noise reduction have also been included. Due to the large sheet resistance of polysilicon, the parasitic gate resistance of the first-stage MOS devices can contribute considerable thermal noise if not minimized through proper layout \([15]\). This involved minimizing the number of squares of polysilicon through custom device layout. The width of the polysilicon parasitic resistance is set by the gate length. However, the length of the parasitic resistance is determined by the gate width and can be reduced to an arbitrarily small size by breaking the gate width into many smaller segments and connecting them in parallel with shared source and drain regions in between. In addition, each gate segment is contacted with metal on both sides. RC lowpass filters were placed at the gates of the cascode devices M2 and M3 and at the gates of the 18-mA cascoded current source to prevent noise from their bias circuits from coupling into the signal path. RC lowpass filters were also placed in each head cell at the gates of the MR bias current passgate/cascode device M6 and the $gm$, feedback passgate device to prevent noise coupling from the head select logic.

### IV. EXPERIMENTAL RESULTS

The CMOS preamplifier design was fabricated in a 0.8-\(\mu\)m CMOS process. The die size was 1.78 x 1.78 mm\(^2\) and the power dissipation was 340 mW with $I_{\text{dc}} = 10$ mA. The preamplifier gain and bandwidth were measured using a network analyzer, and the preamplifier noise was measured using a spectrum analyzer.

The measured preamplifier gain is shown in Fig. 12. The passband gain is about 43 db, or 141 V/V, which is about 30% lower than the nominal simulated gain of 200 V/V. Simulation with process corners suggest that process variations could account for this reduced gain. The gain for both the first and second stages is proportional to $gm r$ where process variations in $gm$ and $r$ do not track. Some of this variation could have been reduced by making the second-stage gain a ratio of resistors by degenerating the input differential pair to this stage. However, this would have required a larger second-stage load resistance, thus reducing the preamplifier bandwidth. Degenerating was not an option for the first stage, where a much larger gain-bandwidth product is needed. Better gain tracking could have resulted if
constant $g_m$ biasing had been used [14]. However, for our prototype we wanted to monitor and predict total current consumption fairly accurately due to our total power budget. Another alternative, which has less circuit complexity, is to keep the current gain stages and make the second-stage load resistance programmable to compensate for the gain variation. The highest programmable load resistance needed to cover all process conditions would still be much less than that with the degeneration method.

The measured preamplifier bandwidth in Fig. 12 is 273 MHz, which is slightly lower than the goal of 300 MHz. To show the bandwidth of only the preamplifier, no discrete inductance was placed in series with $R_{\text{mr}}$ to model the parasitic interconnect inductance $L_{\text{mr}}$, which will be present in the real system. The bandwidth was found to be degraded by a layout and bonding issue. Mainly, the source of each input device M1 was wire bonded to the package though only one bond wire. The parasitic inductance of the bond wire and package, effectively source degenerating the input transistor M1 at higher frequencies. To increase the bandwidth, a double bond pad and two bond wires can be used to reduce the parasitic inductance and increase the $R/L$ pole frequency. Also, the jagged appearance of Fig. 12 at high frequencies is believed to be test-setup related.

Fig. 13 shows the measured preamplifier output noise with the inputs shorted. Equation (16) shows that by shorting out $R_{\text{mr}}$, the total output noise is simply the preamplifier voltage noise. Dividing this output noise by the preamplifier gain of 141 V/V gives an input-referred voltage noise of 0.57 nV/$\sqrt{\text{Hz}}$, which meets the goal of 0.6 nV/$\sqrt{\text{Hz}}$. However, the measured result is higher than the simulated voltage noise of 0.477 nV/$\sqrt{\text{Hz}}$ shown in Fig. 8. This difference is believed to be due to short-channel effects which cause excess thermal noise in MOS devices with short gate lengths [16], [13], [17]. For short channel devices, the noise increases with increasing $V_{\text{th}}$ as well [16], [13]. For this design, the main noise contributor M1 was biased just barely in the saturation region with a low $V_{\text{th}}$. This may explain why the excess noise measured in this work is on the low end of the range cited in the literature. Unfortunately, these short-channel effects are not yet included in most simulation models, including those used for this design.

The measured output noise with an $R_{\text{mr}}$ value of 35 \Omega and an $I_{\text{mr}}$ of 10 mA is shown in Fig. 14. Dividing this by the gain gives an input-referred noise of 1.02 nV/$\sqrt{\text{Hz}}$. Of this, the $R_{\text{mr}}$ contributes 0.761 nV/$\sqrt{\text{Hz}}$. Solving for $i_{\text{mpc}}$ in (16) and plugging in the known variables, the input-referred current noise is calculated to be 10.54 pA/$\sqrt{\text{Hz}}$ for $I_{\text{mr}} = 10$ mA, which is just slightly over the design goal of 10 pA/$\sqrt{\text{Hz}}$.

Table II compares our measured results to those found in the literature for previous CMOS disk drive preamplifiers. In all cases, other than the recently published [4], the work presented here [5], [6] shows improvement by achieving higher bandwidth and lower noise with comparable gain. We note that [4] has similar performance to our design except that the input current noise is approximately 50% higher for the same current level. We attribute our lower current noise to our unique source degeneration technique.

| TABLE II
| COMPARISON OF EXPERIMENTAL RESULTS |
|---|---|---|---|---|
| Gain (dB) | This Work | [1] | [2] | [3] | [4] |
| Bandwidth (MHz) | 273 | 50 | 30 | 120 | 300 |
| Input referred voltage noise (nV/$\sqrt{\text{Hz}}$) | 0.57 | 0.65 | 2 | 1.83 | 0.5 |
| Input referred current noise (pA/$\sqrt{\text{Hz}}$) | 10.54 | 22 | no $R_{\text{mr}}$ | – | 14.23 |
| $I_{\text{mr}}=10$ mA | $I_{\text{mr}}=10$ mA | thin-film PA | $I_{\text{mr}}=10$ mA |
| Min gate length ($\mu$) | 0.8 | 1.2 | 3 | 0.5 | 0.5 |
| Supply voltage (V) | 5 | 5 | 5 | 3.3 | 5 |
V. CONCLUSION

In this paper, we have presented the design for a 455-Mb/s CMOS-only MR preamplifier realized in a 0.8-μm CMOS process. The CMOS-only design provides performance that is comparable to BiCMOS designs at a lower price. This work shows that CMOS preamplifiers can achieve the same level of performance as the more expensive BiCMOS preamplifiers.

This paper introduced a new scheme to reduce current noise below that contributed by a single MOS device. This technique has the potential for even more impact for future submicron processes. We also showed that voltage amplifiers offer lower noise than transimpedance amplifiers for similar gain and bandwidth constraints. The performance of future preamplifiers could be improved by dissipating more power in the first stage or by simply converting the design to a smaller geometry CMOS process.

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REFERENCES


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