CAPACITIVE VOLTAGE MULTIPLIERS:
A High Efficiency Method to Generate Multiple On-Chip Supply Voltages

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ABSTRACT
The use of variable and multiple power supplies to reduce overall power consumption for digital circuits and the need for separate power supplies for mixed analog-digital circuits have been well documented. High efficiency capacitive voltage multipliers can be used to generate multiple and variable on-chip power supplies. Previous literature has presented individual capacitive voltage multiplier designs but has not presented an overview of the design space (i.e., the complete topology list) nor have they provided a method for selecting the best topology for each application. In this paper we identify a complete family of capacitive voltage multiplier modes. We then trim the complete list to a list of recommended modes using a set of heuristic rules. Six of these recommended modes are new and have not appeared in previous literature. We also develop a general set of performance equations for capacitive voltage multipliers that allows us to select and design the best topology for any particular application. We review the effects of parasitic resistance and capacitance and develop new simplified methods to approximate the impact of parasitic capacitances. To verify the validity of our design equations we fabricated and tested a set of sample designs. There is extremely good matching between measured and predicted performance. All the capacitive voltage multiplier modes developed in this paper have either better or as good as the performance of previously presented designs.

1. INTRODUCTION
The use of variable and multiple power supplies to reduce overall power consumption for digital circuits and the need for separate power supplies for mixed analog-digital circuits have been well documented [15-21]. In fact, it has been shown that though the power dissipation for digital circuits reduces with lower power supply voltages, the power dissipation for analog circuits (for a constant signal-to-noise ratio) increases with lowered power supply voltages [21]. Therefore, the ideal solution for a mixed-signal solution would be to generate a low supply voltage for the digital portion of the chip and a higher supply voltage for the analog portion of the chip. Capacitive voltage multipliers (CVMs) are circuits composed of capacitors and switches that is used to convert power from an input voltage to an output voltage. Like inductor based voltage converters the output voltage is not constrained and may be higher than or of a different polarity than the input voltage. However, unlike inductors it is feasible to integrate high quality, reasonable value capacitors and switches in traditional CMOS processes allowing for completely integrated solutions. CVMs are compact, extremely efficient and are ideally suited for low power CMOS integrated circuits.

In this paper each pattern of connecting capacitors and switches together to form a CVM will be referred to as a CVM mode. Each CVM mode has an input terminal (Vin), an output terminal (Vout), and a ground reference terminal (Gnd) as shown in Figure 1 below. CVMs use capacitors to transfer charge from Vin to Vout. These capacitors will be referred to as bucket capacitors. Often a large capacitor is attached to Vout in order to maintain Vout at a constant voltage. This large capacitor will be referred to as a tank capacitor. The bucket capacitor connections move between Vin and Vout in a repetitive pattern. Each step of this repetitive pattern will be referred to as a phase and a complete set of phases will be referred to as a cycle. The cycle will repeat at a constant frequency (f). The average current sourced by Vin will be referred to as Iin and the average current supplied to Vout will be referred to as Iout.

Figure 1 A General Capacitive Voltage Multiplier

2. HEURISTIC RULES
There are an infinite number of ways that capacitors and switches can be combined together to form a CVM. The following set of heuristic rules was used in order to limit which combinations of capacitors and switches were evaluated. The rules were selected based on the requirement that the desired CVM topologies were to be implemented in a CMOS integrated circuit with a minimum number of capacitors and switches. Although these rules are tailored to find solutions for a particular design environment, the solution set derived can be used in different design environments.

Only three terminal designs are considered (Vin, Gnd, Vout)
- All bucket capacitors are the same size
- All bucket capacitors move together as one group
- All bucket capacitors are in series or in parallel
- A cycle is composed of 2 phases (φ1, φ2)
- All three terminals are used during each cycle

Using these heuristic rules the following list of 12 possible phases can be generated. Each one of these phases is represented by a three letter group. The first and last letters indicate which two terminals the bucket capacitors are connected between (i.e. I = Vin, O = Vout, G = Gnd). The middle letter indicates if the capacitors are connected in series or in parallel (i.e. S = Series, P = Parallel). For example the letter group ISP represents the bucket capacitors connected in series between Vin and Gnd.

This list of 12 possible phases can then be used to generate a list of all 96 possible modes. Each mode is composed of two phases and is represented by using two sets of phase letter groups. For example an IPO-OSG has the bucket capacitors in parallel between Vin and Vout during φ1 and in series between Vout and Gnd during φ2. Note that the first letter of the phase code indicates the same side of the bucket capacitors during both phases. For example, in the IPO-OSG mode the side of the capacitors that was towards Vin during φ1 is towards Vout during φ2. The IPO-OSG mode CVM is shown in Figure 2.

Figure 2 IPO-OSG Mode CVM

This list of 96 possible modes can be reduced by applying the heuristic rules and by removing redundant entries. Modes that have
the same two phases but in a different order are equivalent (e.g. IPG-OSI = OSI-IPG). Modes that have the bucket capacitors in series during both phases are similar to modes that are parallel during both phases (e.g. IPG-OP = ISG-OSI). Modes that have the first and second sides of the capacitor group swapped are equivalent (e.g. IPG-PO = GPI-OP). Removing the redundant modes results in the 18 CVM modes:

IPG-IPO  IPG-GPO  IPG-OP  IPG-OGP
IPG-ISO  IPG-GSO  IPG-OSI  IPG-OSG
IPG-OPO  IPG-OPO  IPG-OSI  IPG-OSG
GPO-ISO  GPO-GSO  GPO-OSI  GPO-OSO
IPG-GPO  IPG-OGP

3. CVM PERFORMANCE EQUATIONS

In this section performance equations are developed for the CVM modes described above. These performance equations assume that the CVM is in a steady state condition and that both the input and output voltages have constant DC values. In a typical real CVM the input is driven by a voltage source and the tank capacitor reduces the output voltage ripple to a negligible size. This makes assuming both Vin and Vout to be constants reasonable approximation. These equations also assume that switch resistances and other parasitics are negligible. The impact of parasitics is discussed in Section 5. The equations developed here are generalized for N bucket capacitors.

A CVM can be modeled as a dependent current source, a dependent voltage source and a series output resistance as shown below.

![Figure 5 Ideal CVM Model](image)

Table 1 lists the value of K and Rout for each of the CVM modes in terms of the following variables:

- \( f \) is the frequency at which the CVM cycles
- \( C \) is the size of each individual bucket capacitor
- \( N \) is the total number of bucket capacitors

The IPG-IPO and IPG-GPO modes are not included in this table because they do not transfer power.

The maximum voltage that the CVM can source is:

\[
V_{\text{max}} = K \times V_{\text{in}}
\]  \[1\]

The current that the CVM can source is:

\[
I_{\text{out}} = \frac{V_{\text{max}} - V_{\text{out}}}{R_{\text{out}}}
\]  \[2\]

Iout is zero when Vout equals Vmax. This means that a CVM that is sourcing power has a Vout that is less than Vmax. Rout is inversely proportional to both \( f \) and \( C \). This means that the output power capability of a CVM can be linearly scaled by changing the cycle frequency or the size of the bucket capacitors.

\[
I_{\text{out}} = f \times C
\]  \[3\]

The ratio of Iout to In is the constant:

\[
I_{\text{ratio}} = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1}{K}
\]  \[4\]

The power efficiency (\( \text{Peff} \)) of the CVM is given by equation [5]

\[
\text{Peff} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}}}{V_{\text{max}}}
\]

This shows that the power efficiency of a CVM is a linear function that approaches 100% as Vout approaches Vmax. It also shows that the power efficiency of a CVM composed of nearly ideal components is not always 100% and is not determined by the switch resistances. For a CVM this means that power efficiency will reach an optimal point when the switch resistances are small enough to allow complete energy transfer during each phase. Increasing the switch size beyond this point will only decrease power efficiency by adding unwanted parasitics to the circuit.

4. PREFERRED CVM MODES

Some of the CVM modes listed above are less optimal than other modes that generate the same Vmax. For example the IPG-OSI mode CVM with \( N = 1 \) has a value of K = 2. The IPG-OSG mode CVM with \( N = 2 \) has the same value of K and hence has the same Vmax and Iratio. However, in order to achieve the same Iout the IPG-OSG mode requires four times as much total bucket capacitance. The IPG-OSG mode also requires twice as many bucket capacitors and approximately twice as many switches.

Table 2 shows a list of CVM mode pairs. The first CVM of each pair is the preferred mode. The preferred mode generates the same Vmax as the corresponding mode while using one less bucket capacitor. The preferred mode will also have an Iout that is \( (N+1)/N \) times larger than the corresponding mode for the same clock frequency and bucket capacitor size.

Table 1 CVM Model Parameters

<table>
<thead>
<tr>
<th>MODE</th>
<th>K</th>
<th>Rout</th>
<th>Recommended</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPG-OSI</td>
<td>( N+1 )</td>
<td>( \frac{N}{f \times C} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-GSO</td>
<td>( N )</td>
<td>( \frac{N}{f \times C} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-OPI</td>
<td>( \frac{N+1}{N} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>ISG-OPI</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-OGP</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-OPO</td>
<td>( \frac{1}{2} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>ISO-OPO</td>
<td>( \frac{1}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>ISG-GPO</td>
<td>( \frac{1}{N} )</td>
<td>( \frac{1}{f \times C} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-GPO</td>
<td>( \frac{1}{N} )</td>
<td>( \frac{1}{f \times C} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-ISO</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C} )</td>
<td>Yes</td>
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<tr>
<td>OPI-OSG</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C} )</td>
<td>Yes</td>
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<tr>
<td>ISG-OPG</td>
<td>( \frac{1}{N} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>ISO-GPO</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPO-ISO</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
<tr>
<td>IPG-OSG</td>
<td>( \frac{N}{N+1} )</td>
<td>( \frac{1}{f \times C \times N} )</td>
<td>Yes</td>
</tr>
</tbody>
</table>

\( f \) is the frequency at which the CVM cycles, \( C \) is the size of each individual bucket capacitor, \( N \) is the total number of bucket capacitors, \( P_{\text{in}} \) is the input power, \( V_{\text{out}} \) is the output voltage, and \( V_{\text{max}} \) is the maximum voltage that the CVM can source.

The power efficiency (\( \text{Peff} \)) of the CVM is given by equation [5].

I-509
Table 2 CVM Mode Comparisons

<table>
<thead>
<tr>
<th>Preferred</th>
<th>Corresponding</th>
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<tr>
<td>CVM MODE</td>
<td>CVM MODE</td>
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<tr>
<td>IPO-OSG</td>
<td>IPO-OSG</td>
</tr>
<tr>
<td>IPO-OPI</td>
<td>IPO-OPI</td>
</tr>
<tr>
<td>ISO-OSG</td>
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<tr>
<td>IPG-OSO</td>
<td>IPG-OSO</td>
</tr>
<tr>
<td>IPG-ISO</td>
<td>IPG-ISO</td>
</tr>
</tbody>
</table>

5. NON-IDEAL COMPONENTS

The CVM equations developed in Section 3 assumed that the CVM was nearly ideal, meaning that there are no significant parasitic inductances, resistances or capacitances. This section investigates how and to what extent parasitics affect CVM performance. CMOS transistors that are used as switches have an associated resistance. In Section 3 it was shown that as long as complete charge transfer occurs the power efficiency of the CVM is not impacted by the switch resistance. As the switch resistance is increased the RC time constant of the system will increase. Once the RC time constant becomes large enough the approximation of complete charge transfer will no longer apply. If resistance is the only parasitic considered, increasing the resistance will reduce Iout but will not impact the power efficiency. This is because under steady state conditions the current in to and out of a bucket capacitor must be equal. This means that the Iratio and hence the Eff of the CVM is independent of the parasitic resistance. However, in order to overcome the reduction in Iout due to the parasitic resistance the CVM requires more cycles to transfer the same amount of energy. This increase in cycle count will increase losses due to other parasitics. So increasing parasitic resistance can increase other parasitic losses.

Another significant parasitic associated with CVMs is parasitic capacitance. The CMOS transistors have parasitic capacitances that are proportional to their size. Increasing transistor size to reduce parasitic resistance will increase parasitic capacitance. Bucket capacitors that are located on chip have a significant parasitic capacitance to the substrate. This parasitic capacitance scales with bucket capacitor size and can not be made insignificant. Off chip bucket capacitors have a parasitic capacitance associated with the bond pads. The bond pad capacitance can be made less significant by increasing the bucket capacitance size. These parasitic capacitances can strongly affect CVM performance.

Exactly calculating the impact of a parasitic capacitance is cumbersome. One method to estimate the impact of a parasitic capacitance is to assume that the CVM node voltages and bucket capacitor charge transfers are unaffected by the parasitic capacitance. By using this assumption only the additional charge transfers due to the parasitic capacitance need to be calculated. Because the node voltages are known calculating these parasitic charge transfers is simple.

The impact of parasitic capacitors can become very significant when Vout approaches Vmax. This is because the charge transferred by the bucket capacitors approaches zero at this point while the charge transferred by the parasitic capacitor can be at a maximum.

6. EXAMPLE DESIGNS

In order to verify the equations developed in this paper a number of sample CVM designs were completed [14]. For each design the ideal performance and impact of parasitics was calculated. The sample designs were fabricated using a 1.5µM CMOS process. Calculated, simulated and measured performance all agree well. However, due to space limitations results for only one of the designs is included here. As an example we show simulation and measurement results for an IPO-OSG mode CVM (shown earlier in Figure 2) with N = 2. This design has a 5V Vin, 100KHz cycle frequency and 10µF on chip bucket capacitors. It was optimized to supply 3mA of output current at 2.4V Vout.

The optimal mode for any application is selected by first listing all the modes whose Vmax has the same sign as the desired Vout and has a magnitude of Vmax that is larger than Vout, where Vout is the desired maximum output voltage and Vmax is the maximum voltage that can be generated by the CVM mode. Next, since the efficiency is given by Vout/Vmax (equation [5]) we then find the mode that has the lowest Vmax that is greater than Vout. For our design that gives us three choices OPI-OSG, IPO-OPG and ISO-OPG. Of these three IPO-OPG and ISO-OPG are likely to have a higher efficiency (max =96%) than OPI-OSG due to their lower Vmax (2.5 Volts). However, with Vout so close to Vmax, for the other two modes, the current sourcing ability is much lower. Therefore, for the same Iout required we have to use a larger capacitor. Using the Rout equations in Table 1 for these modes, it can be shown that the bucket capacitor size for the IPO-OPG mode is 5X and for the ISO-OPG is 5X that required for the OPI-OSG. Therefore, for this design example we have decided to sacrifice efficiency for smaller on-chip capacitors and selected the OPI-OSG mode. A higher efficiency design at the cost of larger area would have resulted if the IPO-OPG mode had been selected. However, it should be remembered that a larger on-chip capacitor is likely to have a proportionally larger parasitic bottom plate capacitor. Therefore, the actually realized efficiency is likely to be 5 to 10 percent lower than the theoretical maximum value.

The microphotograph for the complete circuit including on-chip capacitors is shown in Figure 3. The die area occupied by the complete circuit is 130µm by 300µm. The layout and measurement results are shown in Figures 4 and 5. As described in equation 5 the power efficiency is only given by the ratio Vout by Vmax. From Table 1 we see that the Vmax = (2/3)X 5V = 3.3 V. Therefore, we expect the CVM to source zero current when Vout is 3.3 volts and linearly increase Iout for lower Vouts. The simulation and measured Iout vs Vout is shown in Figure 4. It should be noted that the efficiency is affected quite strongly by the choice of input and output voltages. For example, the same mode design that steps down a 3.3 volt input to a 2.0 volt output is likely to have a maximum 91% efficiency. The Iout vs Vout graph shows the linear reduction of Iout. This curve is most accurate for small values of Iout where the MOS switches do not saturate and limit Iout.

Without parasitic capacitances the ratio of Iout/ln = Iratio should be fixed and be given by 1/K which is equal to 1.5 for our design. However, if parasitic capacitances are accounted for then Iratio is likely to decrease as Vout approaches Vmax because Iout has decreased and the parasitic losses are now a larger percentage of Iout. In Figure 5 we present I ratio vs. Vout. As expected both predicted and measured Iratio decreases with increased Vout. The predicted efficiency without parasitics at 2.4 volts output is 73%, with parasitics included is 69.1% and the measured efficiency is 65.4%. The primary parasitic loss mechanism is due to parasitic bottom plate capacitance of the bucket capacitors that are charged and discharged at each clock cycle. The 5% discrepancy between measured and predicted (including parasitics) efficiency can easily accounted for by normal process variations.
8. CONCLUSIONS

Previous literature has not used a systematic approach to identify a complete family of CVM modes or present a generalized set of CVM performance equations. This paper identified a complete family of CVM modes though the use of heuristic rules. Six of these modes have not been found in previous literature. A generalized set of equations was developed for this family of CVM modes including equations for $I_{out}$, $I_{out}$, $I_{out}$, $V_{max}$ and $P_{eff}$. One subset of the CVM (preferred) modes was shown to deliver better performance than their corresponding modes. These preferred modes have the same $V_{max}$ while using one less bucket capacitor and generate a larger $I_{out}$. The effects of parasitic resistance and capacitance were reviewed. Parasitic resistance was shown to reduce $I_{out}$ but not to directly affect $P_{eff}$. A method for approximating the impact of parasitic capacitances was presented. The performance of the CVM modes found in the other literature was compared to the performance of equivalent CVMs presented in this paper. In all cases the performance of the other CVMs was less optimal. The family of CVM modes and generalized equations presented in this paper can be used as a comprehensive CVM reference.

CMVs convert an input voltage to an output voltage. The output voltage is not constrained and may be higher than or of a different polarity than the input voltage. CVMs are particularly attractive for integrated circuit environments because it is feasible to integrate high quality, reasonable value capacitors and switches in traditional CMOS processes. CVMs are compact, extremely efficient and are ideally suited for low power CMOS integrated circuits.

9. CONCLUSIONS


K. Asano 9 presents a CVM mode with $K=(N+2)/(2N+2)$. The IPOP-OSG mode CVM can generate a slightly larger $V_{max}$ and a larger $I_{out}$ while using half as many bucket capacitors and switches. Another limiting factor of the Asano CVM is that for small $V_{out}$ voltage ratios an internal node in the CVM is driven to a negative voltage. B. Pless, J. Ryan, et al. [5][6] both present a dual output CVM mode with $K = 2/3$ and $1/3$. The IPOP-OSG mode CVM can generate these same outputs while using less than half as many switches, one less capacitor, and generating 12.5% more Iout. D. Squires [8] presents two other dual output CVM modes with $K = 2/3$ and $1/3$. The IPOP-OSG mode CVM can generate these same outputs while using fewer phases and generating 150% more Iout.

F. Suzuki et al. [9] presents a CVM mode with $K = N(N+M)$ that use N times M total bucket capacitors. An example with $N = 2$ and $M = 3$ is given. The IPOP-OSG mode CVM can generate slightly larger $V_{max}$ and a 20% larger Iout while using one third as many bucket capacitors and switches. Another limiting factor of the Suzuki CVM is that for small $V_{out}$ voltage ratios an internal node in the CVM is driven to a negative voltage.