A Digital DFT Technique for Verifying the Static Performance of A/D Converters

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Abstract—We present a reconfiguration DFT methodology for evaluating the static performance of a charge redistribution analog-to-digital converter. During the test mode, we reconfigure the ADC to operate as an capacitor ratio converter and measure the primary capacitor ratios which determine the transition voltages. Based on these estimated transition voltages the static performance of the converter under test can be derived. To validate the methodology we designed and fabricated a 11-bit charge redistribution ADC with the reconfiguration DFT technique in a 1.2\textmu m CMOS process. The technique was used to reconstruct the integral (INL) and differential non-linearity (DNL) errors using a digital only tester. The INL and DNL results were verified with analog/digital bench equipment.

I. INTRODUCTION

As the level of integration increases a larger percentage of ASIC now have some analog circuits on them. Data converters, in particular, the successive approximation analog-to-digital converter (ADC) is a popular circuit in many of these mixed-signal ICs. Unfortunately, largely digital circuits with any analog content are required to use mixed-signal testers which are more expensive, adding to the overall manufacturing cost. In order to mitigate this problem we have developed a reconfigurable design-for-test (DFT) technique that uses an all digital tester to verify the performance of analog-to-digital converters. In this paper we apply this technique to a switched-capacitor based successive approximation ADC.

The proposed technique is based on the fact that the transfer function of switched capacitor circuits is primarily determined by capacitor ratios. In successive approximation ADCs the bit transition voltages (i.e., input analog voltages at which the digital value changes) is directly a function of capacitor ratios. In addition, any deviation of those transition voltages (due to parametric capacitor mismatch) is directly related to the performance of the converter. Therefore, by measuring the appropriate capacitor ratios we can estimate the input-output transfer function of the converter [1].

During the test mode, the charge redistribution ADC is reconfigured to operate as an analog-to-digital capacitor-ratio-converter (ADRC) and all the necessary capacitor ratios, are measured. These capacitor ratios are then used to reconstruct the input-output transfer function. The reconstructed transfer function can then be used to predict integral nonlinearity (INL), differential nonlinearity (DNL) and other ADC static performance parameters. We can use these predicted values to determine whether or not the converter meets performance specifications. Dynamic performance parameters are a function of capacitor ratios and other dynamic issues such as settling time and amplifier poles. Therefore, the technique introduced here would also target many dynamic performance parameters, i.e., those that depend on capacitor ratios. In order to validate the technique, we designed, fabricated and tested a 11-bit charge redistribution converter with an embedded ADRC in a 1.2\textmu m CMOS process.

The rest of this paper is organized as follows. In Section II, we describe the new DFT methodology. In Section III we provide experimental results from our fabricated designs. Lastly, we provide some conclusions in Section IV.

II. SYSTEM ARCHITECTURE

The system architecture for the reconfigured charge redistribution converter during both normal and test mode operation is shown in Figure 1. The majority of the analog building blocks such as the amplifier, the comparator, and switches and capacitors are shared during both normal and test mode operation. As will be seen in Figure 7 the majority of silicon area for such converters is devoted to the analog building block, in particular to the capacitor array. Ensuring that we share the analog building blocks during normal and test modes allows us to minimize the area overhead and also minimizes the impact on performance. The primary overhead is limited to digital control logic blocks and some switches. A single control line (TM in Figure 1) determines the mode of operation: TM = 1 indicates test mode and TM = 0 indicates normal mode.

A. Charge Redistribution ADC

The operation of the charge redistribution ADC consists of two sequential modes: sample-and-hold, and bit-cycling. During the sample-and-hold mode, the bottom plates of the input capacitor array \( (C_{1a}, C_{1b}, C_2, \ldots, C_{2N-1}) \) are charged to \(+V_{in}\) and \(-V_{in}\). During the bit cycling mode, all the capacitors of the array (starting from the largest one to the smallest one) are alternately switched to \( \pm V_{ref} \) to generate the transition voltages, \( V_{total,1}, V_{total,2}, \ldots, V_{total,\#V_{ref}} \), where \( V_{total} = (C_{2N-1} + C_{2N-3} + \cdots + C_{1b} + C_{1a}) \). These transition voltages are then sequentially compared with the analog input as illustrated by equations (1) and (2), thereby determining the digital bit from the most significant bit (MSB) to least significant bit (LSB).

\[
V_{X_+} - V_{X_-} =
-2V_{in} + \frac{b_1C_{2N-1} + b_2C_{2N-2} + \cdots + b_4C_{1a}V_{ref}}{C_{2N-1} + C_{2N-2} + \cdots + C_{1b} + C_{1a}}
\]

\[
b_i = \begin{cases} 1, & V_{X_-} - V_{X_+} > 0 \\ 0, & V_{X_-} - V_{X_+} \leq 0 \end{cases}
\]
During the sample-and-hold mode block “A” behaves as a operational amplifier and provides a virtual ground at the top plates of the input capacitor array. However, during the bit-cycling mode it needs to behave as a comparator. In our design block ‘A’ is realized as a fully differential Miller compensated two stage OTA. During the comparison phase a switch in series with the compensation capacitor is disconnected to increase its speed [2]. In our design we follow the amplifier/comparsor (preamp) with a high speed regenerative latch to provide good logic levels and higher comparison speed. The switch control block (modified-SAR) generates the necessary signals to cycle through the input capacitor array.

B. Capacitor Ratio Measurement

During the test mode, the converter is reconfigured to operate as a modified ADCRSC so that it can measure the capacitor ratios of interest in the circuit [3]-[5]. For clarity purposes we have redrawn the circuit in Figure 1 in Figure 2 during the test mode. Considering only the positive half of the circuit for simplicity, we can write an expression for the output of the amplifier \( V_{out} \) at the end of \( n \) clock periods is given by equation 3.

\[
V_{out}(1) = \frac{C_{21}}{C_f} V_{ref} + \frac{C_{2n}}{C_f} V_{ref} (-1)^{D_0(0)} + V_{out}(0)
\]

\[
V_{out}(2) = \frac{C_{21}}{C_f} V_{ref} + \frac{C_{2n}}{C_f} V_{ref} (-1)^{D_0(1)} + V_{out}(1)
\]

\[
\vdots
\]

\[
V_{out}(n) = \frac{C_{21}}{C_f} V_{ref} + \frac{C_{2n}}{C_f} V_{ref} \sum_{i=0}^{n-1} (-1)^{D_{0}(i)} + V_{out}(0)
\]

Equation (3) can be rearranged in the form shown in equation (4). Here we note that the average digital output after \( n \) clock periods provides an estimate of the desired capacitor ratio \( \frac{C_{2n}}{C_{2m}} \), plus an error term, \( \epsilon_n \), that can be made extremely small by increasing \( n \) [6].

During the test mode a switch array is necessary to reconfigure the capacitors to be located either in the forward or in the feedback path to select the specific capacitor ratios to be measured. Figure 3 shows the switching scheme that decides which capacitors are required to be in the forward or feedback path. For example, as shown in Figure 3, to measure the capacitor ratio \( \frac{C_{2n-1}}{C_{2m}} \), the capacitor \( C_{2n-1} \) needs to be in the forward path and all the other capacitors need to be in the feedback path. This is simply done by connecting the switch \( S_1 \) to the forward path and connecting the other switches to the feedback path.

C. Fault Model

In this paper we focus on parametric faults that are introduced due to process variations. We assume that catastrophic faults due to defects have been address by alternate methods. To illustrate our fault model and the impact of process variations we shall use a 3-bit converter as an example. During normal mode of operation the transition voltages are defined by capacitor ratios whose ideal values are \( \frac{1}{2}, \frac{1}{4}, ..., \frac{1}{8} \) and \( \frac{1}{16} \). However, due to process variations the actual capacitor ratios are randomly distributed [7]. Due to process variations the capacitor ratio \( \frac{C_{2n}}{C_{2m}} \) is equal to \( \frac{1}{2}(1 + \epsilon_1) \), where \( \epsilon_1 \) is small random value. Similarly, \( \frac{C_{2n}}{C_{total}} \) and \( \frac{C_{2m}}{C_{total}} \) are \( \frac{1}{2}(1 + \epsilon_2) \) and \( \frac{1}{2}(1 + \epsilon_3) \). These errors in capacitor ratios affect the transition voltages. For example, the transition voltage for ‘100’ no longer occurs at \( V_{in} = \frac{V_{ref}}{2} \) but occurs at \( V_{in} = \frac{V_{ref}}{2} (1 + \epsilon_1) \). The transition for the digital word ‘100’ is not the only one affected by this error. Every transition in which the MSB is ‘1’ is affected by this fault. However, this parametric fault does not affect any of the transition voltages for \( V_{in} < \frac{1}{2}(1 + \epsilon_1) \), i.e., the MSB is ‘0’. In general, process variations affect all the capacitor ratios therefore we need to extend this analysis to the multiple fault case. Single faults in each of the capacitor ratios are independent of each other. We can therefore consider the multiple fault case as a superposition of such single faults. We illustrate the impact of both single and multiple faults in Table 1 on the transition voltages for a 3-bit converter [4]. These transition voltages characterize the overall transfer function of the data converter. The static performance of the converter under test can be estimated by reconstructing the transfer function based on precisely measured capacitor ratios. This analysis can easily be extend to any arbitrary \( n \)-bit converter without any loss of generality.

D. ADCRSC Resolution Requirements

In the next section we provide measurement results from a fabricated 11-bit successive approximation converter. Before we present these results we evaluate the resolution requirements for the ADCRSC to accurately reconstruct the converter performance during normal operation. To evaluate ADCRSC requirements we focus on reconstructing traditional performance metrics such as integral nonlinearity error (INL) and differential nonlinearity error (DNL) from estimated capacitor ratios. Here we are interested in evaluating the fault coverage and test yield of the test process as a function of the ADCRSC resolution.
TABLE I

TRANSITION VOLTAGE LEVELS WITH MULTIPLE FAULTS

<table>
<thead>
<tr>
<th>Bit word</th>
<th>Transition voltage with multiple faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>$V_{ref} + (1 + e_1)$</td>
</tr>
<tr>
<td>010</td>
<td>$V_{ref} + (1 + e_2)$</td>
</tr>
<tr>
<td>011</td>
<td>$V_{ref} + (1 + e_1) + V_{ref} + (1 + e_2)$</td>
</tr>
<tr>
<td>100</td>
<td>$V_{ref} + (1 + e_1)$</td>
</tr>
<tr>
<td>101</td>
<td>$V_{ref} + (1 + e_1) + V_{ref} + (1 + e_3)$</td>
</tr>
<tr>
<td>110</td>
<td>$V_{ref} + (1 + e_3) + V_{ref} + (1 + e_2)$</td>
</tr>
</tbody>
</table>

TABLE II

ADCRC RESOLUTION REQUIREMENTS

<table>
<thead>
<tr>
<th>A/D Res.</th>
<th>ADCRC Res.</th>
<th># of Runs</th>
<th>$P_C$ (%)</th>
<th>$P_{GF}$ (%)</th>
<th>$P_R$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11bit</td>
<td>12bit</td>
<td>500</td>
<td>62.6</td>
<td>96.5</td>
<td>100</td>
</tr>
<tr>
<td>11bit</td>
<td>13bit</td>
<td>500</td>
<td>62.2</td>
<td>28</td>
<td>96.8</td>
</tr>
<tr>
<td>11bit</td>
<td>14bit</td>
<td>500</td>
<td>60.2</td>
<td>12</td>
<td>96.5</td>
</tr>
</tbody>
</table>

If the converter's performance specifications are within acceptable bounds then the circuit is regarded as being fault-free. For these experiments we specify that a converter whose maximum $DNL$ and $INL$ are less than 0.5$V_{LSB}$ and 0.75$V_{LSB}$ is considered to be fault-free. The exact values of these acceptable thresholds are application-dependent but our choice of numbers are fairly typical. Fabricated capacitor ratios are affected by a number of process variations and typically have a Gaussian distribution whose variance is inversely proportional to capacitor area [7]. In particular, for our design presented in the next section we have used a rather small unit capacitor size (0.05$pF$) so random variations are larger and visible even in a small test set size. For small capacitances, local edge effects dominate and the relative error can be written as, $\Delta V = K C^{-3/4}$ [7]. A value for $K = 1.057 \times 10^{-12}$ was extracted from measured data in [8]. The value above suggests that a 0.05$pF$ capacitor should provide a 1% matching which is consistent with other measurements as well. Note, we use this expression only as a guide to derive the resolution requirements for the ADCRC.

For this experiment we use 500 hundred Monte Carlo runs within MatLab to evaluate the ADCRC requirements for our 11-bit converter. Table II shows the fault coverage achieved for different ADCRC resolutions. In this table $P_C$ represents the initial yield, $P_{GF}$ represents the probability that a good IC will fail the test, and $P_R = P_{BF}/P_B$ is the fault coverage of the test process, i.e., the probability that a bad circuit fails the test. From Table II we note that ADCRC resolutions between 12-bit to 14-bit provide good fault coverage. However, the test yield increases with improved resolution. Recall that the 1st order ADCRC used here is based on a incremental data converter, i.e., one additional bit of resolution requires twice the number of clock cycles [1]. With that in mind, we suggest that either a 13-bit or 14-bit ADCRC resolution would be good compromise between test time and test yield.

III. MEASUREMENT RESULTS

To validate the DFT technique we designed and fabricated a 11-bit successive approximation A/D with the ADCRC switching logic built on-chip. A Xilinx 9500 series CPLD was used to implement the up-down counter for the ADCRC and to implement the digital comparator used to find the transition voltages during normal mode operation. During normal production test these functions could be programmed into the digital production tester. As mentioned earlier, we used a relatively small unit capacitor size of 0.05$pF$ to exaggerate the mismatch so that even with a small test size we would encounter parametric variations.

Figure 4 shows the digital output from the fabricated chip captured via a digital oscilloscope while measuring capacitor ratios of 1/2 and 1/16 during the test mode. Table III shows all the capacitor ratios measured during the test mode using 13-14 bits of precision. For this experiment the count was stopped whenever the total number of ‘1s’ was 8192. This method reduces the total measurement time and increases the resolution as we measure a smaller ratio. The last column in Table III shows the worst case error due to finite quantization in the ADCRC.

In Figure 5 we compare the INL of the original converter measured using bench equipment and the reconstructed virtual INL. In this
figure the X-axis shows the digital output value and the Y-axis shows the error in virtual LSBs (VLSBs), where 1 VLSB corresponds to 1 LSB. We use the term VLSB due to the virtual reconstruction of the data converter using our DFT technique. We see that in general the reconstructed INL closely matches the actual measured INL. However, they are not exact. The difference is most visible at the midpoint and at the higher end of the digital output. However, the error is always bounded by 1/2 LSB. In a similar fashion, in Figure 6 we compare the DNL of the original converter measured using bench equipment and the reconstructed virtual DNL. Once again there is some deviation between the original DNL and the reconstructed DNL. However, once again the error is always less than 1/2 LSB.

The validity of the reconfiguration DFT test technique introduced in this paper is clearly visible in the results presented above. However, it is important to note the limitations of the technique as well. The basic principle of the DFT technique is based on the idea of using a 'tester' (the ADCRC) that can provide higher resolution than the CUT (the successive approximation converter). However, it is also important to note that reconfiguration process itself changes the circuit adding some small but finite errors. The difference between the actual measured results and the reconstructed results shown in Figures 5 and 6 are partially a result of the finite quantization error but is also partially attributable to noise and parasitics introduced by the reconfiguration process, i.e., the additional analog switches added for reconfiguration. The technique is clearly viable for resolutions for 11-bits and less but should be used with some degree of caution for verifying the operation of much higher resolution data converters.

The Figure 7 shows the microphotograph of the fabricated chip (2.2mm × 2.2mm). The top portion of the die contains the analog circuits including the amplifier, bias, comparator, etc, the middle portion consists of the capacitor and switch array and dedicated routing area, and the bottom portion contains the digital control logic, respectively.

IV. CONCLUSIONS

In this paper, we presented a reconfiguration DFT technique to detect parametric faults in a charge redistribution ADCs. The static performance and many dynamic performance parameters of the charge redistribution ADC is primarily determined by capacitor ratios. To validate the technique a 11-bit converter was fabricated in an 1.2µm CMOS process and tested. As part of the verification process, the INL and DNL are derived from the estimated transition voltages during the test mode and compared with those measured during normal mode using bench-top equipment.

REFERENCES