A CMOS High Efficiency +22 dBm Linear Power Amplifier

Yongwang Ding
Bermai Inc., Minnetonka, MN 55305, USA
Email: yding@bermai.com, Tel: (952) 960-1105

Ramesh Harjani
University of Minnesota, Minneapolis, MN 55455, USA
Email: harjani@ece.umn.edu, Tel: (612) 525-4032

Abstract—Modern wireless communication systems require power amplifiers with high efficiency and high linearity. CMOS is the technology of choice for complete systems on a chip due to its lower costs and high integration levels. However, in the past it has always been difficult to integrate high efficiency power amplifiers in CMOS. In this paper we present a new class of operation (parallel A&B) for power amplifiers that improves both their dynamic range and power efficiency. A prototype design of the new amplifier was fabricated in a 0.18μm CMOS technology. The measurement results show over 44% PAE and +22 dBm output power. In comparison to a normal class A amplifier, this new design increases the P1dB by over 3 dB and yet reduces DC power consumption by up to 50% in the linear operation range.

I. INTRODUCTION

CMOS power amplifiers (PA) are used in modern radios primarily because they integrate well with digital circuits. Many linear power amplifiers have been designed for integrated radios [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], and can be categorized as class A, class B, and class AB according to the duty cycle of the their drain currents [11].

Figure 1 shows a simplified circuit diagram for a CMOS cascode power amplifier. Differential designs are often preferred for their improved power supply rejection ratio (PSRR) and suppression of even order harmonics. The input transistors M1 and M3 are biased to a fixed voltage, V\text{indec}, through a pair of large valued resistors, R\text{indec}. The cascode transistors M2 and M4 provide isolation between the input and output nodes. Capacitor C\text{ac} is an AC coupling capacitor, RFC is the RF choke and L\text{0} and C\text{p} are used for output matching. This basic topology can be made to operate in different modes, e.g., class A mode, class B mode, etc., by altering the input DC bias voltage V\text{indec} to this amplifier.

Class A amplifiers are used where linear operation and high gain are critical. However, there is not matching class A output throughout the input signal range such amplifiers need to be biased at a relatively high level. With the result that class A amplifiers consume significantly higher DC power than other amplifier topologies even for low input signal levels.

Class AB amplifiers have a drain current duty cycle that lies between class A and class B amplifiers. It should be noted that even class A amplifiers will eventually operate in class AB mode when the input signal level is sufficiently high.

Most CMOS power amplifiers are operated in class AB mode for higher output power and better power added efficiency (PAE) [1], [3], [4], [5], [7], [9], [10], [8], [12]. It is possible to achieve over 40% PAE at the maximum output power for real life CMOS class AB amplifiers. However, as the DC power consumption of such amplifiers is relatively constant over the entire operation range, its PAE becomes much smaller when the output power is lower than the maximum level. This becomes a serious problem for systems that have large dynamic-range (i.e., high peak-to-average ratio), such as multi-carrier OFDM (802.11a/802.11g) systems. For example, for the 802.11a standard 54 Mbps operation (64 QAM), the power amplifier needs to be backed off by 8 to 10 dB from its output P1dB point. With the result that during normal operation the PAE effectively reduces to the 5% range.

CMOS class B amplifiers have the benefit of being able to self-adjust the DC power consumption depending on the input power level. Therefore, the PAE of a CMOS class B amplifier is much higher than that of a class A or class AB amplifier at small input levels. However, the gain of such amplifiers changes with the input signal level resulting in more distortion than either class A or class AB amplifiers.

This paper presents a new power amplifier with a parallel combination of a class A/AB amplifier and a class B amplifier. This amplifier provides the high linearly of a class A amplifier while providing the PAE of a class B amplifier over the entire operating range.

II. CMOS PARALLEL CLASS A&B AMPLIFIER

A parallel combination of a class A and a class B amplifier can be used to improve both the linear operation range and the power efficiency. A conceptual block diagram for such an amplifier is shown in Figure 2. As will be shown later the outputs from both the amplifiers are combined in the current domain with little overhead. As both amplifiers are operating in parallel we call this a parallel class A&B amplifier. In the rest of this section we derive individual characteristics of each of the amplifiers and the combined parallel class A&B amplifier.

The transconductance for a class A amplifier is given by Equation 1, where, W and L are the channel width and length of the input transistor respectively, V\text{od} = V\text{indec} - V\text{th}, is the over drive voltage, and \(g_m\), shown in equation 2 is a measure of velocity saturation effect, and E\text{sat} is the saturation field...
strength. The transconductance of the class A amplifier is constant until the input or the output compresses.

\[ g_{mA} = \mu_n C_{ox} \frac{W}{L} V_{od} \left( 1 + \frac{1}{2} \rho_a \right) \left( 1 + \rho_a \right)^{-\frac{3}{2}} \]  

(1)

\[ \rho_a = \frac{V_{od}}{L \cdot E_{sat}} \]  

(2)

For a MOSFET operated in class B mode, the drain current is not constant, therefore, large signal analysis has to be applied to calculate the effective transconductance. The transconductance of a CMOS class B amplifier can be calculated by using the expression in Equation 3, where, \( I_{d,fund} \) is the drain current at the fundamental frequency and \( V_{in} \) is the amplitude of the input signal.

\[ g_{mB} = \frac{I_{d,fund}}{V_{in}} \]  

(3)

The drain current at the fundamental frequency, \( I_{d,fund} \), of a CMOS class B amplifier with a sinusoid input of \( V_{in} \cdot \sin(\omega t) \) is given by Equation 4.

\[ I_{d,fund} = \frac{2}{T} \int_0^T I_d(t) \sin(\omega t) \, dt = \frac{2}{T} \int_0^T \frac{1}{2} \mu_n C_{ox} W \frac{V_{in}^2}{L} \frac{\sin^2(\omega t)}{1 + \rho_b \sin(\omega t)} \sin(\omega t) \, dt \]  

(4)

where, \( \rho_b \) is given by

\[ \rho_b = \frac{V_{in}}{L \cdot E_{sat}} \]

From Equations 3 and 4 we can derive the transconductance of a class B amplifier as shown in Equation 5. We note that the transconductance increases with the input signal level until it reaches the compression point.

\[ g_{mB} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{in} \left[ \frac{1}{2 \rho_b} \frac{1}{\pi} \frac{1}{\rho_b^2} + \frac{1}{\rho_b} \right] - 4 \frac{1}{\pi \rho_b^2 \sqrt{1 - \rho_b}} \arctan \left( \frac{\sqrt{1 - \rho_b}}{\sqrt{1 + \rho_b}} \right) \]  

(5)

When the input is very small, the transconductance of the class B amplifier can be approximated by Equation 6.

\[ g_{mB} \bigg|_{V_{in} \rightarrow 0} = \frac{2}{3} \frac{\mu_n C_{ox} W}{L} V_{in} \]  

(6)

From Equation 6, it is clear that the effective transconductance and resulting power gain of a class B amplifier increases with increased input amplitude. However, class A and/or class AB amplifiers start to compress rapidly as the input signal levels increase. So, in a parallel class A&B amplifier the class A amplifier is the primary transconductance contributor at low signal levels, however, the class B is the primary contributor at high signal levels. With the result that the class B amplifier can compensate for the gain compression of the class A amplifier when they are appropriately combined. This is shown in Figure 3. In this figure, the solid line with the squares shows the power transfer characteristics for the parallel class A&B amplifier. The dashed line with the 'x's shows the contribution from the class A amplifier while the dashed line with the diamonds shows the contribution from the class B amplifier. As can be seen, at low input levels the class A amplifier contributes the majority of the gain as the class B amplifier gain is very low. As the input level increases the gain of the class B amplifier increases and its contribution to the overall gain increases proportionately. When the input level is sufficiently high, the class B amplifier provides the majority of the power gain and compensates for the gain compression of the class A amplifier.

In Figure 3, we see that the class B amplifier compensates for the gain compression of the class A amplifier so we expect a higher P1dB for the parallel class A&B amplifier in comparison to a class A amplifier alone. Additionally, since the class A amplifier does not have to provide significant power gain at larger inputs it can be designed to be smaller and biased at a lower level, i.e., resulting in an improved PAE. To evaluate both the PAE and the linearity characteristics we have designed and simulated three amplifiers, class A, class B and parallel class A&B, all of which drive low impedance loads so that gain compression occurs at the inputs rather than at the outputs.
The linearity characteristics are shown in Figure 4 and the PAE curves are shown in Figure 5 for the three amplifiers. Figure 4 shows the fundamental and intermodulation signals (IM3) for all three amplifiers. Also marked on the figure is the signal-to-distortion ratio (SDR) for all three amplifiers. In the parallel class A&B amplifier the class A contributes to the majority of the gain at low signal levels so we expect the linearity to be similar to a class A. Interestingly, we find that the IM3 products are 5 to 7 dB lower than even the class A amplifier. This is because the class B amplifier partially compensates for the distortion caused by the class A amplifier. At high signal levels the class B amplifier contributes the majority of the output power, at which point the total distortion of the parallel class A&B amplifier is dominated by the class B part and is larger than that of the class A amplifier. Multicarrier systems such as 802.11a/802.11g are very sensitive to power amplifier distortion. In particular, 54 Mbps operation for either of these standards requires a minimum SDR of 25 dB. The higher linearity of the parallel class A&B PA allows it to transmit 54Mops signals at 10dBm output power while the class A amplifier with a SDR of 19 dB would only be able to support a 36 Mbps stream at the same output power.

Figure 5 shows the power added efficiency (PAE) for the three power amplifiers vs. input signal power. We see that the PAE of the class A amplifier is lower than both the class B amplifier and the parallel class A&B amplifier due to the higher DC bias. In the parallel class A&B amplifier the class A and class B portions of the structure contribute to the output power differently at different input signal levels. For this reason, at low input levels the PAE is comparable to a class A while at higher input levels the PAE approaches that of a class B. The parallel class A&B amplifier provides an ideal compromise between gain, output power and power added efficiency.

For these graphs we have used a low output impedance to ensure that the power amplifier compresses at the input rather than at the output. However, in practice power amplifiers are usually limited at both the input and the output. If compression occurs at the output then the mode of operation of the transistor will have limited impact on the performance. Therefore, in practice the difference between the parallel class A&B amplifier and the class A/AB amplifiers maybe not be as large as shown in Figure 4 and Figure 5. But the improvements offered by the combined structure are still significant as will be seen in the next section.

III. EXPERIMENTAL RESULTS

In this section we present a prototype design of the parallel class A&B amplifier in the UMC 0.18μm RF CMOS technology and compare its performance with other state-of-the-art CMOS power amplifiers. A simplified circuit diagram of the differential parallel class A&B power amplifier design is shown in Figure 6.

Shunt inductors $L_{sh}$ are used to match the inputs, and the inductors $RFC$ are used as RF chokes to prevent coupling of the RF signal to the power supplies. An additional pair of inductors $L_o$ is used to match the output port. The input transistors, M2 and M4, have aspect ratio of (768/0.18) and are biased at the edge of the threshold voltage via the two large value resistors, i.e. $V_{indch} \sim V_{th}$. These two transistors form the transconductors for the class B amplifier. The other two input transistors, M1 and M3, have an aspect ratio of (192/0.18) and are biased well above the threshold voltage.
so that they operate in saturation for the majority of the input range, i.e. $V_{\text{indc}} \sim V_{\text{th}} + V_{\text{od, max}}$. These two transistors form the trawinators for the class A amplifier. The size of the class A transistors M2 and M4 are only one quarter the size of the class B transistors M1 and M3. This is because the class B transistors do the "heavy lifting" at large input signals. The cascode transistors have an aspect ratio of (1200/0.34). These transistors have a thicker gate oxide with a higher breakdown voltage than the input transistors and are able to handle the large voltage swings at the outputs. A microphotograph of the fabricated power amplifier is shown in Figure 7.

The output power, PAE and gain results for the parallel class A&B amplifier is shown in Figure 8. The linear power gain is 12 dB, the maximum output power is over +22 dBm and the maximum PAE is over 44%. The amplifier reaches its P1dB at an output level of +20.5 dBm and the PAE at P1dB is 36%.

In Table 1 we provide measured results for prototype amplifier and compare it with other CMOS class AB power amplifiers [3], [10], [4]. The new amplifier has a higher power added efficiency. This is particularly visible when the amplifiers are operated in their linear operating range, i.e., 4dB to 8dB back-off, that is usually mandated by system requirements. For example at 8dB back-off the PAE of the parallel class A&B amplifier is over 50% higher than the other designs. This can result in significant reduction in DC power consumption for similar RF output power levels.

**IV. CONCLUSIONS**

In this paper we have presented a design for a new power amplifier with a parallel class A&B structure. This new amplifier provides superior performance in terms of both linearity and power efficiency in comparison to previous designs. Measurement results show 12 dB power gain (single stage), 22 dBm output power and more than 44% PAE. More importantly this circuit uses significantly less DC power at 4 or 8 dB back-off in comparison to other class AB amplifiers.

**ACKNOWLEDGEMENTS**

The authors thank A. Shaw for measurement help, and N. Lemay, P. Cheung, M. Batenhoff and J. Harvey for helpful discussions.

**REFERENCES**


