Designing LC VCOs Using Capacitive Degeneration Techniques*

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In this paper, we present a detailed analysis of VCOs using a capacitively degenerated negative resistance cell. The negative resistance cell using capacitive degeneration has a higher maximum attainable oscillation frequency and a smaller equivalent shunt capacitance when compared to the widely used cross-coupled negative-gm cell. These properties are of particular interest for the design of high-frequency and/or wide tuning range VCOs. The negative resistance provided by a traditional capacitively degenerated negative resistance cell is lower than that provided by a cross-coupled negative-gm cell. We present an active capacitive degeneration topology that overcomes this limitation. To validate this circuit topology we use two test vehicles. The first test vehicle is a 5.3 GHz VCO designed in a 0.25 μm CMOS technology and the second test vehicle is a 20 GHz VCO designed in a 0.25 μm BiCMOS technology. Measurement and simulation results from both test vehicles effectively demonstrate the efficacy of the capacitive degeneration technique.

Keywords: Voltage-controlled oscillators; analog integrated circuits; BiCMOS integrated circuits; capacitive degeneration; high-frequency LC oscillators; negative resistance cell.

1. Introduction

Integrated LC voltage-controlled oscillators (VCOs) are critical building blocks in high-performance communication systems. The ever-increasing demand for bandwidth places very stringent frequency, power and noise requirements on such systems. Significant research effort has been put into improving the noise and power performance of integrated LC VCOs. The majority of this effort is targeted at optimizing the LC tank and the negative resistance cell design [1]-[11]. And, bulk of this work is based on the topology using cross-coupled negative resistance cell. The integrated cross-coupled negative resistance cell has been used widely for its simplicity and easy differential implementation. A transistor that has capacitive

*Portions of this manuscript and material referred in this manuscript have appeared in [18], [19], and [20].
degeneration can also produce negative resistance. The basic discrete frequency dependent negative resistance cell based on capacitive degeneration has been used previously in [13]- [16], and recently, examples of integrated differential implementations have been presented in [17]- [19] without extensive description of the operating principles and/or comparison with the cross-coupled negative-\(g_m\) cell. This paper analyzes the performance and limitations of the different negative resistance cells including the impact of different process technologies.

One of the interesting focus of investigation is the high-frequency behavior of the different negative resistance cells. Even for the widely used cross-coupled negative-\(g_m\) cell, there has been very little work on its behavior at frequencies close to the unity current gain frequency, \(f_T\), of the process. Only recently has the maximum attainable oscillation frequency of this topology been presented [12]. The analysis in this paper covers different aspects of the underlying physical mechanisms that limit the high-frequency performance of \(LC\) VCOs to provide in-depth design insights for the circuit designers. The analysis considers not only the negative resistance cells but also the design techniques for low-power and low-noise implementations including buffers and driven loads. The analysis shows that, with proper design, the negative resistance cell using capacitive degeneration can out-perform the widely used cross-coupled negative-\(g_m\) cell especially at high-frequencies. Another focus of investigation is the equivalent capacitance of the negative resistance cells. This study shows the wide tuning capability of the VCO using a capacitively degenerated negative resistance cell that accrues from its low equivalent capacitance. A design example of a wide tuning range 5.3GHz VCO in 0.25\(\mu m\) CMOS technology is provided.

These investigations motivated us to develop a new negative resistance cell topology that can further improve the performance in comparison to previous topologies. The proposed cell is based on the capacitively degenerated topology, but unlike the designs in [17], [18], and [21], it uses two cross-coupled active devices that serve as the degenerating capacitance and also provide additional transconductance. To show the effectiveness of the presented negative resistance cell using an active capacitive degeneration, Section 3.2 presents the design and experimental results for a 20GHz VCO in IBM SiGe 0.25\(\mu m\) BiCMOS process, and provides a comparison of its performance with previously reported 20GHz \(LC\) oscillators. This paper also discusses some practical design considerations including the issue of common-mode oscillation and techniques to prevent it, and methods to utilize the small equivalent capacitance of the negative resistance cell to either improve phase noise or increase output signal swing.

2. \(LC\) Tank-based VCO Design

Fig. 1 shows a simplified circuit model for a parallel \(LC\) oscillator in steady state, where the resistance \(R_P\) represents the tank loss, \(R_{Eq}\) is the effective negative resistance generated by the active devices, and \(C_{Eq}\) is the effective shunt capacitance
contributed by the active devices in the negative resistance cell. For sustained oscillation, the magnitude of the effective negative resistance $|R_{Eq}|$ has to be smaller than $R_p$. Additionally, for high-frequency operation where $C_{Var}$ is small, the effective capacitance $C_{Eq}$ should be small compared to $C_{Var}$ so as to not limit the maximum attainable oscillation frequency and tuning range.

The traditional cross-coupled cell which is also known as the negative-$g_m$ cell is used widely due to its simplicity and its ability for differential signaling. First of all, we investigate the limitations of the traditional cross-coupled cell in both BiCMOS and CMOS form. We then analyze the maximum attainable frequency of oscillation and show the importance of the base/gate resistance and the equivalent parasitic capacitance ($C_{Eq}$) of a negative resistance cell. All simulations comparing BiCMOS and CMOS use either the 0.25 $\mu$m IBM SiGe BiCMOS process or the 0.18 $\mu$m TSMC CMOS process. Though comparisons between process technologies is never exact, these two processes are comparable with similar $f_T$s. Next, we discuss the negative resistance cell using capacitive degeneration. The analysis uses a CMOS example and focuses on the resulting benefits from the small equivalent capacitance ($C_{Eq}$) of the cell. Lastly, we present a negative resistance cell using an active capacitive degeneration that further improves the performance of the negative resistance cell using a simple capacitive degeneration. The design issues related to this new architecture are discussed using a BiCMOS implementation example. The issue of common-mode oscillation is discussed at the end of this section.

For the rest of this section, we use small-signal models for the behavioral analysis of the different negative resistance cells. Even though small-signal analysis is insufficient to completely predict the large-signal behavior of an oscillator, it still provides designers with good insight and compares fairly well with the simulation results, suggesting the appropriateness of this approach.

2.1. Maximum Attainable Oscillation Frequency for the Cross-Coupled Negative Resistance Cell

In this section we evaluate the maximum frequency of oscillation for a given power budget for BJT and MOS implementations of the cross-coupled structure. Several factors (negative resistance cell design, buffer stage bandwidth, frequency tuning range and the parasitic capacitances of the constituent components) affect the maximum oscillation frequency. Due to its higher transconductance for a given current,
the BJT implementation provides a better $R_{Eq}$. However, as will be shown later, the finite base resistance severely limits the maximum attainable oscillation frequency.

2.1.1. Negative resistance cell

We first consider the mechanisms that degrade high-frequency performance in a cross-coupled negative resistance cell. Veenstra [12] derived expressions for the maximum attainable oscillation frequency for a BJT cross-coupled cell using small-signal analysis. We use a simpler method that provides better physical insight into the degradation mechanisms. Fig. 2 shows simplified circuit schematics for the (a) BJT-based and (b) CMOS-based cross-coupled cells, (c) the shunt equivalent $R_{Eq} \parallel C_{Eq}$ model, and (d) the differential small-signal model for the BJT version. At low frequencies, $R_{Eq}$ is approximately $-2/g_m$ where $g_m$ is the device transconductance. Typically BJTs have a higher $g_m$ than CMOS transistors for a given bias current and are a better choice for low power design. Additionally, the low flicker noise corner makes BJT devices better candidates for low-power low-noise oscillator designs. But, with increasing frequency, the magnitude of $|R_{Eq}|$ becomes large and eventu-
ally flips over and $R_{E\text{q}}$ becomes positive. This is primarily due to the non-negligible base resistance, $r_b$, at high frequencies.

At high frequencies, the impedance offered by the base-emitter capacitance $C_\pi$ becomes comparable to $r_b$ as a result a larger portion of the base voltage appears across $r_b$ rather than $C_\pi$. Additionally, there is a phase difference between the voltage across $C_\pi$ and the base voltage due to the resistor-capacitor voltage division. The voltage across $C_\pi$ can be calculated using the small-signal model shown in Fig. 2 (d). Using the voltage division ratio ($v_\pi/v_{in}$), we can define an effective transconductance:

\[ G_{m,\text{eff}} \equiv \frac{v_\pi}{v_{in}} \equiv A g_m \]  

(1)

In Fig. 2 (d) the difference between the transconductor current and $i_\pi$ is returned to the signal source, thereby generating a negative resistance. A relationship between the current $i_\pi$ and the transconductance associated with this current ($g_\pi$) is given by $g_\pi \equiv i_\pi/v_{in}$. Only the real parts of $G_{m,\text{eff}}$ and $g_\pi$ contribute to the equivalent negative resistance. Therefore, $R_{E\text{q}}$ can be approximated as:

\[ R_{E\text{q}} \approx \frac{-2}{\text{Re}[G_{m,\text{eff}}] - \text{Re}[g_\pi]} \]  

(2)

Equation (2) suggests that $R_{E\text{q}}$ degrades rapidly as $\text{Re}[g_\pi]$ approaches $\text{Re}[G_{m,\text{eff}}]$, and has a distinct corner frequency which will be revisited later. An expression for the negative to positive transition frequency of $R_{E\text{q}}$ ($\omega_{\text{tran}}$) can be calculated by considering the condition $\text{Re}[G_{m,\text{eff}}] - \text{Re}[g_\pi] \leq 0$, which results in:

\[ \omega_{\text{tran}} = \sqrt{\frac{1 + \frac{r_b}{r_\pi}}{r_bC_\pi^2}} \left( g_m - \frac{1}{r_\pi} \right) \]  

(3)

Assuming $r_b/r_\pi \ll 1$, $r_\pi = \beta/g_m$ and $\beta \gg 1$ where $\beta$ is the base to collector current gain, then equation (3) can be simplified to:

\[ \omega_{\text{tran}} \approx \sqrt{\frac{\omega_T}{r_bC_\pi}} \]  

(4)

where $\omega_T = g_m/C_\pi$. For the MOS version of the cross-coupled structure, $r_b$ and $C_\pi$ are replaced with $r_g$ and $C_{gs}$. Equation (4) shows that the transition frequency is a strong function of the bias current, device size and base resistance. In the case of the MOS transistor, a multiple finger layout can be used to drastically minimize gate resistance [22]. The relatively high base resistance of the BJT in comparison to the gate resistance of the CMOS device can result in a lower transition frequency, despite its higher $\omega_T$. Fig. 3 (a) shows the simulated $R_{E\text{q}}$ and $C_{E\text{q}}$ for the BJT and MOS cross-coupled cells using the 0.25 $\mu$m BiCMOS and 0.18 $\mu$m CMOS technologies respectively at a bias current of 2 mA. We see that the BJT-based design shows a smaller $|R_{E\text{q}}|$ than its CMOS counterpart at low frequencies due to its higher transconductance value. However, it has a much lower transition frequency ($\sim 28$ GHz) as compared to the CMOS case ($\sim 53$ GHz). Fig. 3 (b) shows plots for
Fig. 3. Negative resistance for the cross-coupled cell (a) simulation and (b) model.

$|R_{Eq}|$ for the BJT and MOS cross-coupled structures using equation (2). We see that equation (2) predicts a transition frequency that is higher than seen in the simulation results. This is primarily because we neglected the emitter resistance, base-collector capacitance, and emitter-collector capacitance and resistance in our analysis. But more importantly, it correctly predicts the rapid degradation of $R_{Eq}$ after the corner frequency. Increasing the bias current increases $\omega_T$, the transition frequency. This implies that a low base (gate) resistance design is important not only from a noise perspective but also from a low-power perspective. This analysis suggests that careful layout is imperative to increase the transition frequency, especially for the CMOS case where the gate resistance can be reduced substantially by appropriate layout techniques without any serious impact on $\omega_T$ and/or $C_{gs}$.

2.1.2. Buffer stage design

Another important factor that impacts the maximum attainable frequency of oscillation is the buffer stage. Buffer stages are usually implemented as emitter followers because of their high input impedance and wide bandwidth. Fig. 4 shows the simplified circuit schematic for the VCO core coupled with a buffer. The input admittance,
Fig. 4. Emitter follower buffer stage schematic.

\[ Y_{BI} = \frac{1}{Z_L \left[1 + \frac{r_\pi}{1 + j\omega C_\pi r_\pi} \left(g_m + \frac{1}{Z_L}\right)\right]} \]  

(5)

When the load impedance is resistive, \( Z_L = R_S \), the effective input shunt resistance and capacitance looking into the buffer are given by equations (6) and (7).

\[ R_{Eq,BI} = R_S \frac{1 + \beta \left(1 + \frac{1}{g_m R_S}\right)^2 + \left(\beta \frac{\omega}{\omega_T}\right)^2}{1 + \left(\frac{\omega_T}{\omega}\right)^2 \left(1 + \frac{1}{g_m R_S}\right)^2} \approx R_S \left[1 + \left(\frac{\omega_T}{\omega}\right)^2 \left(1 + \frac{1}{g_m R_S}\right)^2\right] \]

(6)

\[ C_{Eq,BI} = C_\pi \frac{\frac{g_m R_S}{r_\pi} + \frac{1}{R_S^2}}{\left[1 + \frac{1}{r_\pi \left(g_m + \frac{1}{R_S}\right)}\right]^2 + \left(\omega C_\pi r_\pi\right)^2} \approx \frac{1}{\omega_T R_S \left(1 + \frac{1}{g_m R_S}\right)^2 + \left(\omega T\right)^2} \]

(7)

If we assume that \( \beta \gg 1 \) and \( \omega \approx \omega_T \), then we can make the approximations shown in equations (6) and (7). It is essential that \( R_{Eq,BI} \) is large enough so as to not reduce the loaded \( Q \) of the tank, while \( C_{Eq,BI} \) is small enough so as to not limit the frequency tuning range. In many integrated transceiver designs the buffer drives an internal capacitive load, \( C_L \). In this case the effective shunt resistance and capacitance looking into the buffer input are as follows:

\[ R_{Eq,BI} = -\frac{(1 + g_m r_\pi)^2 + \omega^2 r_\pi^2 (C_\pi + C_L)^2}{\omega^2 r_\pi C_L (g_m r_\pi C_\pi - C_L)} \]  

(8)

\[ C_{Eq,BI} = \frac{(1 + g_m r_\pi) C_L + \omega^2 r_\pi^2 C_\pi C_L (C_\pi + C_L)}{(1 + g_m r_\pi)^2 + \omega^2 r_\pi^2 (C_\pi + C_L)^2} \]  

(9)

Equation (8) predicts a negative input resistance at the buffer input when \( g_m r_\pi > C_L/C_\pi \). This condition is easily met as \( g_m r_\pi (= \beta) \) can easily be greater than ten. This additional negative resistance provided by the buffer can be utilized by the VCO core when driving a capacitive load. Fig. 5 shows the small-signal model for the VCO core and buffer load. The combined negative resistance is equal to
Fig. 5. Parallel LC oscillator model including buffer stage impedance.

$R_{Eq} || 2R_{Eq,B1}$. The negative resistance provided by the buffer reduces the $g_m$ requirement of the cross-coupled cell, and hence can be used to reduce power consumption and noise. Equation (9) predicts that the effective shunt capacitance is smaller than $C_\pi$ or $C_L$ which allows for a high-frequency design with wider tuning range. This basic negative resistance seen in the buffer due to capacitive emitter degeneration will be used to build a new negative resistance cell for the VCO in the following sections.

The impedance looking at the output of the buffer, $Z_{BO}$, determines the bandwidth of the buffer. In a common base configuration, the output impedance is equal to $\sim 1/g_{m,buffer}$ at low frequencies. However, when driven by a high impedance oscillator, $Y_{OSC}$ affects $Z_{BO}$ as shown in Fig. 4. The output impedance for this configuration is given by:

$$Z_{BO} = \frac{Z_\pi + Z_{OSC}}{g_{m,buffer}Z_\pi + 1} \tag{10}$$

where $Z_\pi = (1/sC_\pi \parallel r_\pi)$ and $Z_{OSC} = 1/Y_{OSC}$. In Figure 6 we show circuit and bias details for MOS and bipolar oscillator cores. The oscillator admittance, $Y_{OSC}$ is a strong function of $Z_{biasL}$ and $Z_{biasC}$ as well as $Y_{BI}$. Nevertheless, because the real part of $Z_{BO}$ tends to increase with an increasing base impedance, we can derive an optimistic pole frequency produced at the emitter of the buffer stage given by:

$$\omega_{pole} = \frac{g_{m,buffer}}{C_L} \tag{11}$$

This pole frequency has to be higher than the oscillation frequency to prevent output signal attenuation. More importantly, the signal suffers fairly large phase shift around the pole frequency, and relatively small process variations can introduce large phase shift between two output signals when the pole frequency is close to the oscillation frequency. In Fig. 7 we plot the pole frequency, $\omega_{pole}$ as a function of the load capacitance $C_L$ at the output of the buffer stage for bipolar and MOS implementations at a 1mA bias current. The MOS design has a lower pole frequency even with a relatively small load capacitance due to its lower $g_m$. This implies that even though the MOS cross-coupled cell can provide a negative resistance up to very
Fig. 6. Oscillator output admittance examples for (a) BJT, (b) MOS VCOs.

Fig. 7. Pole frequency vs. load capacitance of the buffer stage.

high frequencies, the smaller bandwidth of the buffer stage can limit the practical maximum attainable oscillation frequency.

2.1.3. Parasitic capacitance and tuning range

Another important factor that determines the maximum attainable oscillation frequency for a given technology and power budget are the parasitic capacitances of the various components. The maximum oscillation frequency of the circuit in Fig. 1 is $1/\sqrt{L(C_{Fiz} + C_{Eq})}$. When a desired tuning range, $\Delta \omega$, is required, the maximum attainable center frequency can be described as:

$$\omega_{Max} = \frac{1}{(1 + \frac{\text{Tune}}{200}) \sqrt{L_{Min} (C_{Fiz} + C_{Eq})}}$$ (12)
where $T_{\text{une}}$ is the tuning range which is expressed as a percentage of the center frequency, $L_{M_{\text{in}}}$ is the smallest feasible inductance without suffering severe process variations, $C_{F_{\text{le}}}$ is the fixed sum of parasitic capacitances contributed by the varactor, the inductor, and the buffer, and $C_{E_{\text{eq}}}$ is the effective shunt capacitance of the negative resistance cell. The effective capacitance of the cross-coupled cell is $\sim C_{e}/2$. At high frequencies, this along with the effective capacitance from the buffer stage becomes a significant portion of the overall capacitance and limits the maximum attainable oscillation frequency and tuning range.

In this subsection, we showed the mechanisms that degrade the $R_{E_{\text{eq}}}$ generated by the cross-coupled cell and showed how the effective capacitance from the buffer and negative resistance cell limits the maximum attainable frequency and tuning range. These limitations have motivated a new negative resistance cell, described in the next subsection, that has a higher negative to positive transition frequency and lower effective capacitance thereby enabling low-power low-noise high-frequency design. Even though the new design is technology independent, the benefits are maximized in a BiCMOS implementation, and hence the following sections will focus on a BiCMOS design.
Fig. 10. The small signal model and the equivalent shunt models for the capacitively degenerated negative resistance cell.

Fig. 11. The transition frequency vs. $C_s$.

2.2. Negative Resistance Cell Using Capacitive Degeneration

As seen in the previous section, a capacitive emitter/source degenerated transistor can generate negative resistance. Resonator-based VCOs using this technique have been presented in [13]-[21], and a similar topology has been used in a relaxation oscillator [23]. Fig. 8 shows a single ended negative resistance cell using capacitive emitter degeneration. The $R_{eq}$ and $C_{eq}$ can be described using the formulas in equations (8) and (9). When a voltage is applied to the base, a part of it appears across $C_\pi$, which in turn generates the transconductor current. Portion of this transconductor current is returned to the signal source via the capacitor-capacitor divider. A portion of this returning current has a $180^\circ$ phase shift from the voltage that is applied, which signifies a negative resistance. This negative resistance cell has a very small effective capacitance. First of all, $C_\pi$ and $C_e$ are in series. Second, the $g_{m}$-cell affects the charge buildup across each capacitor and increases the effective $C_\pi$ while decreasing the effective $C_e$, thus further reducing the effective series capacitance. This smaller effective parasitic capacitance compared to that
Fig. 12. Simulated (a) $R_{E_q}$, (b) $C_{E_q}$, and (c) $L_{E_q}$ results.
of cross-coupled negative-\(g_m\) cell, \(\sim C_\pi/2\) and \(\sim C_{gs}/2\) in Bipolar and CMOS respectively, enables the design of wide tuning range VCO. Fig. 9 shows the CMOS implementation of differential negative resistance cells using capacitive degeneration. The negative resistance cell shown in Fig. 9(a) has cross-link. For the negative resistance cell without the cross-link, as shown in Fig. 9(b), the \(LC\) tank can be connected between the gates, and the power supply can be connected to the drains of the transistors. This connection can improve the power supply pulling and supply noise rejection. But, the cell without cross-link is susceptible to common-mode oscillations, and care has to be taken to prevent this from occurring. These mechanisms will be discussed at the following sections. In this section, we focus on the cell with cross-link, but the cell without cross-link shows similar behavior. Because the tank is connected in shunt across the negative resistance cell, an equivalent shunt resistance and shunt reactance model for negative resistance cell is convenient for analysis. Fig. 10 shows the small signal model and the equivalent shunt model of the negative resistance cell using capacitive degeneration. For the negative resistance cell with capacitive source degeneration, the imaginary part of the equivalent shunt impedance can become inductive instead of capacitive. Fig. 10 shows simplified models for both the capacitive and the inductive cases. Equation (13) shows the calculated input admittance, and equations (14), (15) and (16) show the extracted equivalent resistance (\(R_{Eq}\)), capacitance (\(C_{Eq}\)), and inductance (\(L_{Eq}\)) respectively where \(\omega_T\) is \(g_m/C_{gs}\).

\[
Y_{ln} = \frac{1}{2 \left[ g_m^2 + \omega^2 (C_{gs} + C_s)^2 \right]} \times \left\{ -\omega^2 C_s \left( 2C_{gs} + C_s \right) g_m \right. \\
\left. + j\omega C_s \left[ -g_m^2 + \omega^2 C_{gs} \left( C_{gs} + C_s \right) \right] \right\} 
\]  

(13)
\[ R_{Eq} = -2 \frac{1 + \left( \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{C_{gs}}{C_{gs}} \right)^2}{g_m \left( \frac{\omega}{\omega_T} \right)^2 \frac{C_{gs}}{C_{gs}} \left( 2 + \frac{C_{gs}}{C_{gs}} \right)} \]  

(14)

\[ C_{Eq} = \frac{-2 + \left( \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{C_{gs}}{C_{gs}} \right)^2}{2 \left( 1 + \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{C_{gs}}{C_{gs}} \right)^2} \]  

(15)

\[ L_{Eq} = \frac{2 \left( 1 + \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{C_{gs}}{C_{gs}} \right)^2}{\omega^2 C_s \left[ 1 - \left( \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{C_{gs}}{C_{gs}} \right) \right]} \]  

(16)

The imaginary part provides inductive impedance up to a certain frequency and then changes into capacitive impedance. Equation (17) shows the transition frequency where the impedance changes from being inductive to being capacitive.

\[ \omega_{L\rightarrow C} = \omega_T \sqrt{\frac{C_{gs}}{C_{gs} + C_s}} \]  

(17)

Fig. 11 shows the transition frequency as a function of the source degeneration capacitor \( C_s \). As \( C_s \) increases, the transition frequency decreases. For typical value of \( C_s \) and \( C_{gs} \), \( \omega_{L\rightarrow C} \) is about 0.4-0.5 \( \omega_T \). The simulated values for \( R_{Eq} \), \( C_{Eq} \), and \( L_{Eq} \) using small signal analytical calculations are shown in Figs. 12(a), 12(b) and 12(c) respectively. The negative resistance for the proposed structure is smaller than that for a typical cross-coupled negative-\( g_m \) structure, but the difference reduces with increasing \( C_s \). Below the inductive to capacitive transition frequency the effective shunt inductance is fairly large and has minimal effect on the inductance value in the tank. The tradeoff between the reduced negative resistance and effective parasitic capacitance has to be optimized. To compensate for the smaller negative resistance of the proposed structure, the \( g_m \) has to be increased. For a given power budget, this can be done by increasing the transistor size in CMOS. This increases the effective parasitic capacitance, but as long as the increased effective parasitic capacitance of the capacitively degenerated negative resistance cell is less than the effective parasitic capacitance of the traditional cross-coupled negative-\( g_m \) cell, the proposed design is better. Because the \( g_m \) is proportional to the square root of the device size, and the \( R_{Eq} \) is inversely proportional to \( g_m \) for typical structure, we can define a benefit factor, \( B \), as done in equation (18).

\[ B = \frac{1}{R_{ratio} \sqrt{C_{ratio}}} \]  

(18)

where

\[ C_{ratio} = \frac{C_{EQ (New)}}{C_{EQ (Typical)}} \]  

(19)
and

\[ R_{ratio} = \frac{R_{EQ} \text{(New)}}{R_{EQ} \text{(Typical)}}. \]  

(20)

Fig. 13 shows the benefit factor as a function of frequency. The benefit factor is small near \( \omega_T \) but increases sharply with decreasing frequency. This implies that for a given \( -R_{Eq} \) requirement and power budget, the proposed structure has a smaller parasitic capacitance; such that it is capable of a larger tuning range or a larger output swing. However, care should be taken to ensure that too large a transistor size is not selected to limit the actual benefit.

2.3. Active Capacitive Degeneration Based Negative Resistance

Another unique property of the negative resistance cell using capacitive degeneration is a high negative to positive transition frequency of \( R_{Eq} \) as presented in [17]. The presentation in [17] does not explain the physical mechanism for this high transition frequency. The small effective capacitance has a higher impedance than \( C_\pi \) resulting in a smaller effective \( r_g \). This causes the voltage drop across \( r_g \) and the phase shift from the base voltage to the voltage across \( C_\pi \) to be smaller than in the cross-coupled cell. So, it retards the \( R_{Eq} \) degradation mechanism, and increases the \( R_{Eq} \) transition frequency. However, emitter/source degeneration decreases the effective transconductance. Because the \( R_{Eq} \) transition frequency is also a function of \( g_m \), the reduced effective transconductance limits the improvement in the \( R_{Eq} \) transition frequency and also increases the \( |R_{Eq}| \) value. For a given power budget, increasing the device size can compensate the increased \( |R_{Eq}| \) in CMOS technology as shown in the previous section. But in BJT where the \( g_m \) is insensitive to device size to the first order, the increased \( |R_{Eq}| \) requires more current to increase \( g_m \), or a higher \( Q \) tank design, and hence higher \( Q \) inductor design which is not trivial at high frequencies. In this section, we present a further improvement to the capacitively emitter degenerated negative resistance cell in BiCMOS implementation that mitigates the reduction in \( g_m \) issue mentioned here. Fig. 14 shows the evolution of the proposed negative resistance cell. Two capacitively emitter degenerated negative resistance cells are interconnected by using a cross-coupled NMOS pair. The gate and drain of each NMOS device is connected to the emitters of each negative resistance cell respectively. The \( C_{gs} \) of the NMOS device replaces the emitter degenerating capacitor, and two current sources are combined into one as shown in Fig. 14. The cross-coupled NMOS pair works both as emitter degenerating capacitors and also provides additional transconductance to improve the negative resistance value. Fig. 15 shows the equivalent small signal circuit model for the proposed negative resistance cell. The input admittance is calculated to be:

\[ Y_{IN} = \frac{\frac{1}{2} \left[ g_{m2} \left( \frac{r_s}{Z_s} - 1 \right) + \frac{1}{Z_s} \right]}{\left[ 1 + g_{m1} Z'_\pi \right] + \frac{1}{Z_\pi} \left[ g_{m2} \left( \frac{r_s}{Z_s} - 1 \right) + \frac{1}{Z_s} \right]} \]  

(21)
where $Z'_\pi = (r_\pi \parallel 1/sC_\pi)$, $Z_\pi = r_b + Z'_\pi$, $Z_g = r_g + 1/sC_{gs}$, and $g_{m1}$ and $g_{m2}$ are transconductances for the BJT and the NMOS transistor respectively. If we ignore $r_b$ and $r_g$ the equivalent shunt resistance is given by:

$$R_{Eq} = \frac{-2 \left[ \left( \frac{1}{r_{\pi}} + \Delta g_m \right)^2 + (\omega C_T)^2 \right]}{\left( \frac{1}{r_{\pi}} + \Delta g_m \right) \left( \frac{g_{m2}}{r_{\pi}} + \omega^2 C_{gs} C_\pi \right) - \omega^2 C_T \left( \frac{C_{gs}}{r_{\pi}} - C_\pi g_{m2} \right)} \quad (22)$$

where $\Delta g_m = g_{m1} - g_{m2}$ and $C_T = C_\pi + C_{gs}$. For a fixed bias current, the transconductance of the BJT is to first order unaffected by the device geometry, but the transconductance of MOS device increases as the square root of the device size. To find the optimum $g_{m1}/g_{m2}$ ratio, we let $g_{m1} = \delta g_{m2}$, and $g_{m2} = K/\sqrt{C_{gs}}$, where $K$ is a constant. Using this relationship and assuming that $g_{m1} r_\pi \gg 1$ then equation (22) can be simplified to equation (23).

$$R_{Eq} = \frac{-2 \delta \left[ (1 - \delta)^2 + \left( \frac{\omega}{\omega_T} \right)^2 \left( 1 + \frac{\Gamma^2}{\omega_T^2} \right) \right]}{(1 - \delta) g_{m1} \left( \frac{1}{\beta} + \frac{\omega^2 \Gamma}{\omega_T K} \right) - \omega^2 \left( \frac{\Gamma}{\beta K} - \frac{1}{\omega_T} \right) (C_\pi + \Gamma^2)} \quad (23)$$

where $\omega_T = g_{m1}/C_\pi$, and $\Gamma = \delta g_{m1}/K$. In Fig. 16 we plot the expression in equation (23) as a function of $\delta$ for different values of $g_{m1}$. It shows that the $R_{Eq}$ is optimized when $\delta$ is near unity, i.e., $g_{m1} \approx g_{m2}$. Additionally, it shows that this ratio is more critical than the magnitude of $g_{m1}$ itself. For example a 15mA/V-15mA/V combination results in a better $R_{Eq}$ than a 30mA/V-15mA/V combination which gives some important design insights for optimizing the design.

Fig. 17 and 18 show the simulated $R_{Eq}$ and $C_{Eq}$ results for the cross-coupled cell, the simple capacitively degenerated cell, and the proposed active capacitively degenerated cell respectively. All designs use 2mA bias current and use the same BJT size. As predicted the simple capacitive degeneration cell shows a higher $R_{Eq}$ transition frequency but a larger $|R_{Eq}|$ in comparison to the cross-coupled cell. The proposed cell also has a higher $R_{Eq}$ transition frequency in comparison to the cross-coupled cell, but it shows a better $R_{Eq}$ in comparison to the simple capacitively
degenerated cell. This implies that the proposed cell is particularly useful for low-power low-noise design for frequencies above the $R_{Eq}$ transition frequency of the cross-coupled negative-$g_m$ cell. This is because it does not require an increased bias current for a proportional increased $g_m$ which would also increase the noise from the transistor. Fig. 18 shows that the proposed cell has a little higher $C_{Eq}$ in comparison with the simple capacitively degenerated cell between 20GHz and 40GHz, but this value is much smaller than the $C_{Eq}$ of the cross-coupled negative-$g_m$ cell.

The analysis results in Fig. 16 suggest that a BJT-BJT combination would be preferred to a BJT-MOS combination for better $g_m$ matching for the proposed cell. Even though a BJT-BJT combination results in a better $R_{Eq}$, the relatively high $r_b$ of the BJT results in a low $R_{Eq}$ transition frequency and its benefit reduces to
only the small effective capacitance.

2.4. Common-Mode And Differential Mode Oscillation

One distinct difference between the capacitively degenerated cell and the cross-coupled cell is its common-mode behavior. The common-mode input admittance for the ideal cross-coupled cell in Fig. 2 is near zero \((Y_{IN} \approx 0)\). Fig. 19 shows the common-mode equivalent circuit schematic for the capacitively degenerated cell. Unlike the cross-coupled cell, each half circuit of the capacitively emitter-degenerated cell provides negative resistance. For common-mode signals, the emitter degeneration capacitor connected between two emitters in series \((C_S)\) does not have any effect on the common-mode impedance; only the capacitors connected to
the ground act as degeneration capacitors. Therefore, when $C_S = 0$, each half of the circuit has the same effective resistance and capacitance as in the differential mode, i.e. $R_{EqD} = R_{EqC}$ and $C_{EqD} = C_{EqC}$. And in this case, the differential and common-mode admittances can be described as:

$$
R_{EqH} = R_{EqC} = R_{EqD},
C_{EqH} = C_{EqC} = C_{EqD},
Y_{IN,C} = \frac{2}{R_{EqH}} + j\omega 2C_{EqH},
Y_{IN,D} = \frac{1}{2R_{EqH}} + j\omega \frac{C_{EqH}}{2}.
$$

The equations above predict that the common mode $|R_{Eq}|$ is 4 times smaller than the differential mode $|R_{Eq}|$, and common mode $C_{Eq}$ is 4 times larger than the differential mode $C_{Eq}$. It implies that the capacitively emitter degenerated cell is more prone to oscillate in common-mode when $C_S = 0$.

Fig. 20 shows the simulated common-mode and differential mode $R_{Eq}$ for a capacitively emitter degenerated cell where $C_S = 0$. As expected the common mode shows a much smaller $|R_{Eq}|$. When we use this type of negative resistance cell, the
tank bias network has to be carefully designed to prevent common-mode oscillation. Fig. 21 shows the $LC$ tank with a center tapped inductor and capacitor including the bias network. If $Z_{biasL}$ and $Z_{biasC}$ are very small, the common mode impedance to ground becomes $(L/2 \parallel 2C)$. And circuit can now oscillate at $\omega = 1/\sqrt{L(C + C_{eqH})}$ in common-mode. In fact, when $Z_{biasL}$ and $Z_{biasC}$ are zero, each half circuit becomes an independent oscillator, and there is no phase relationship constraint between two output signals. If $Z_{biasL}$ and $Z_{biasC}$ are very large, the common-mode impedance of the tank becomes very large, and the circuit cannot oscillate in common-mode. If the bias network impedance is zero, the circuit prefers to oscillate in common-mode. Thus, a bias network with large impedance converts the oscillation mode from common-mode to differential-mode. Fig. 22 shows the oscillation mode conversion from common mode to differential mode for the same circuit by simply altering the bias network impedance. The differential mode signal is shifted down in this plot for graphical convenience only.

In the proposed negative resistance cell with the cross-coupled MOS pair, the common-mode admittance of the MOS pair is near zero. Only the effective input capacitance of the buffer contributes to the common-mode negative resistance. This makes the proposed cell less susceptible to common-mode oscillations as compared to a simple capacitively emitter degenerated cell.

2.5. Wide Tuning Range

A wide tuning range is often important because it can accommodate more process and temperature variations. For a high frequency oscillator design, the effective capacitance from the negative resistance cell is one of the key factors that limits the tuning range. The proposed capacitively emitter degenerated cell has a small effective capacitance. Fig. 23 graphically shows the mechanism that results in a small effective capacitance. In the cross-coupled negative-$g_m$ structure, the tank looks into the base of $Q2$, the collector of $Q1$, and the base of buffer transistor $Q3$. 

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But in the active capacitively degenerated topology, the tank only looks into the base of Q1. Furthermore, the equivalent capacitance looking into the base of Q1 is much smaller than the $C_\pi$ of Q1 as shown in Section 2.3.

Fig. 24 shows how the effective capacitance of a negative resistance cell affects the oscillator tuning range. For this simulation, a two turn spiral inductor with 740 pH inductance and 17 fF parasitic capacitance, and diode varactors with capacitance range from 28.6 fF to 68.4 fF are used. The tuning range and center frequency go down rapidly with increasing parasitic capacitance of the negative resistance cell. In particular, if we keep the center frequency constant by changing the varactor size, the tuning range reduces even more rapidly as shown in Fig. 24. For example, if the load at the output port in Fig. 23 is 200 fF, the equivalent shunt capacitance looking into the base of Q3 is about 44.4 fF. This parasitic loading causes severe frequency and tuning range limitations for the cross-coupled negative-$g_m$ topology as can be seen in Fig. 24. But in the proposed topology, the equivalent shunt capacitance looking into the base of Q3 functions as part of the emitter degenerating capacitance. And the effective parasitic capacitance loading the tank is further attenuated.
Fig. 24. Simulated tuning range vs. effective capacitance of negative resistance cell.

by Q1.

A small effective capacitance also provides more room to increase the inductor size in the tank. In many cases the $R_p$ of LC tank increases with increasing inductance value [24]. So, a large inductance value enables a large output signal power. Depending on the technology and the design constraint, the $Q$ of inductor can also increase with increasing inductance [25]. In this case, both the increased signal power and improved $Q$ contributed by the small effective capacitance can result in lower phase noise as can be seen in the modified Leeson’s phase noise formula [26] shown in equation (25).

$$L(\Delta f, K_{VCO}) = 10 \log \left\{ \left( \frac{f_0}{2Q \Delta f} \right)^2 \left[ \frac{FkT}{2P_0} \left( 1 + \frac{f_C}{\Delta f} \right) \right] + \frac{1}{2} \left( \frac{K_{VCO}v_m}{2\Delta f} \right)^2 \right\}$$  (25)

where

$L(\Delta f, K_{VCO})$ phase noise in dBC/Hz;
$f_0$ frequency of oscillation in Hz;
$\Delta f$ frequency offset from the carrier in Hz;
$F$ noise figure of the transistor amplifier;
$k$ Boltzmann’s constant in J/K;
$T$ temperature in K;
$P_0$ RF power produced by the oscillator in W;
$f_C$ flicker noise corner frequency in Hz;
$K_{VCO}$ gain of the VCO in Hz/V;
$v_m$ total amplitude of all low frequency noise sources in V/$\sqrt{\text{Hz}}$

The first term within the log in equation (25) predicts a decreased phase noise with increasing tank $Q$ and signal power. This discussion emphasizes that the small effective capacitance of the negative resistance cell is not only advantageous for high frequency and wide tuning designs, but results in additional flexibility during
the LC tank phase noise optimization process.

3. Design Examples

This section presents two design examples of integrated differential VCOs using the capacitive degeneration technique. The 5.3 GHz VCO in the 0.25 μm CMOS technology demonstrates the wide tuning capability of the negative resistance cell using capacitive degeneration. While the 20 GHz VCO in the 0.25 μm SiGe BiCMOS technology illustrates the effectiveness of the negative resistance cell using active capacitive degeneration at high frequencies.

3.1. 5.3GHz VCO in CMOS

The TSMC 0.25 μm CMOS technology has been used to design one 5.3 GHz VCO. Fig. 25 shows the circuit schematic for the VCO. Bias details are not included. Three and half turn inductor providing 3.715 nH of inductance, 4.715 Ω series resistance \( R_S \) and 134.6 fF parasitic capacitance is connected to the drain of each transistor. The equivalent inductor model [27] used in this design is shown in Fig. 26.
At 5.3 GHz the inductor $Q$ is around 15. Assuming the tank $Q$ is dominated by inductor $Q$, the equivalent parallel resistance at resonance frequency is roughly $R_S(1 + Q^2) = 1.1K\Omega$. So the negative resistance cell should have $R_{EQ}$ greater than $−1.1\ K\Omega$ and the design target was $−900\ \Omega$. With 3.715 nH inductance, the required capacitance for 5.3 GHz oscillation is 121 fF. A MOS capacitor has been used as a varactor. A MIM capacitor is inserted between drain and MOScap to apply control voltage. Combined with the MIM cap, the fixed portion of the variable capacitance is 65 fF and the inductor has an equivalent parasitic capacitance of 25 fF at 5.3 GHz. Connecting the buffer to the source of transistor as shown in Fig. 25 removes the effect of buffer parasitic capacitance that is not possible in the typical cross-coupled
negative-$g_m$ structure. Because the source follower buffer offers a capacitive impedance, the complete replacement of $C_s$ with the buffer is possible. The negative resistance cell has been designed to have negligible effective parasitic capacitance. So by fully utilizing the tunable portion of the capacitance, 60 fF, an oscillator centered at 5.3 GHz can be designed with a with a significant tuning range. The effective parasitic capacitance for a cross-coupled negative-$g_m$ cell, exceeding several tens of femto farads, combined with the buffer parasitic capacitance limits the tuning range quite severely, or requires a smaller inductance value that results in reduced output voltage swing (or a higher bias current). A reduced output voltage swing results in deterioration of the phase noise performance.

Using the inductor model implemented in the TSMC 0.25 μm design library, the equivalent parallel resistance versus inductance is calculated and shown in Fig. 27. The equivalent parallel resistance increases with increasing inductance, confirming the possibility of obtaining large output signal swing using the proposed architecture. Fig. 28 shows the tuning range simulation results. The designed 5.3 GHz VCO has 1.14 GHz (21.5%) tuning range. Typical structure VCO has also been designed using the same tank and power budget, and the tuning range is compared with the proposed structure in Fig. 28. Simulation data confirms the improved tuning range and reduced parasitic characteristics of the proposed architecture. The simulated phase noise results for both the proposed structure and the typical structure operating at 5 GHz are shown in Fig. 29. It has $-83.4 \text{ dBC/Hz}$ phase noise at 100 KHz offset and $-106 \text{ dBC/Hz}$ phase noise at 1 MHz offset from 5 GHz.

### 3.2. 20 GHz VCO in BiCMOS

A 20 GHz VCO with 5 GHz tuning range has been designed using the IBM 0.25 μm BiCMOS process. At the time of the initial design, we did not fully appreciate the
importance of the $g_{m1}/g_{m2}$ ratio for $R_{Eq}$ optimization. So unfortunately, in the experimental prototype design the $g_{m1}/g_{m2}$ ratio ($\delta$) is about 0.3 which is less than the optimal value. At 20GHz, the simulated $R_{Eq} \approx -500\,\Omega$ and $C_{Eq} \approx 13\,\text{fF}$. This includes the effect of the buffer. We note that $C_{Eq}$ is about $1/9\,\text{th}$ the $C_s$ of $Q_1$ which is equal to 126 fF. The designed VCO uses a two-stage emitter follower as buffers for each output. The capacitive impedance looking into this buffer works as a degeneration capacitance and contributes to the negative resistance as shown in [17]. But, as described in the previous section, the degeneration using active devices is more desirable and the buffer has been designed to have minimal impact on this design. Two back-to-back junction diodes described in Section 2.5 are used as the varactors, and the anode is connected to the base of the BJT to minimize the N/Substrate parasitic capacitance effect. The spiral inductor uses two turns to generate a 740 pH inductance. A single differential inductor is used for higher $Q$ and to save area. This single inductor design without a center tap also prevents common mode oscillation. The chip microphotograph and VCO layout details are shown in Fig. 30.

For the measurements, we used RF probes to directly connect to the bare die. Single ended measurement setup has been used throughout. Fig. 31 shows the measured output power spectrum of the 20GHz oscillation signal. The measured tuning range is compared with the simulated tuning range in Fig. 32 (a). The measured oscillation frequency is slightly higher than the simulation results. This is because we overestimated the parasitic of the signal lines and probe pads. Measurement results show more than 5 GHz (25%) tuning range. This wide tuning was possible because of the low effective capacitance of the proposed negative resistance cell. Fig. 32 (b) shows simulated oscillation frequency at a fixed bias condition as a function of the temperature for different process corners. For these corner simulations, only the process corner parameter for bipolar devices and 6 sigma variations have been considered. Fig. 32 (b) shows that temperature and process variation results in about
4 GHz variation of the center frequency clearly showing the importance of a wide tuning range design that can tolerate temperature and process variations. The VCO core consumes only 2 mA, and each emitter follower branch drains 0.5 mA from a 4.5 V supply respectively. This low bias current compared to the other presented \( \sim 20 \) GHz VCOs [8]-[11] supports the low-power design capability of the proposed topology. Despite the wide tuning range, the maximum output power variation was less than 3.5 dBm over the whole frequency tuning range as shown in Fig. 33, which is comparable to other presented works. A low power signal close to the noise floor is injected at the opposite side of differential output to remove the random drifting of the free running VCO as shown in Fig. 34 (a). The phase-noise of the injected signal was \(-121 \text{ dBC/Hz}\) at 2 MHz offset from the 19.4 GHz carrier. At high injection levels, the phase noise of the VCO follows the phase noise of the injected signal source. But at low injection power levels, the locking range reduces and the phase noise approaches its intrinsic level as shown in Fig. 34 (b) [28]-[30]. Fig. 35 shows the measured injection locking range as a function of injected signal power and the measured phase noise at an injected signal power of -58dBm. At this injection level the lock range is about 800 KHz. The actual power delivered to the tank is much smaller because of the attenuation through the buffer stage. The phase noise is measured at a 2 MHz offset from 19.4 GHz to eliminate the phase noise attenuation through injection locking. The measured phase noise was \(-105.5 \text{ dBC/Hz}\). Simulations predicted a value of \(-110.6 \text{ dBC/Hz}\). This value is obtained using an NMOS noise coefficient \((\gamma)\) of \(2/3\) and no induced gate noise contribution was included in the simulations. For short-channel devices, \(\gamma\) can reach as high as 2.5, and induced gate noise should be included. Therefore our simulations underestimate the actual phase noise [31]. We believe the 5 dB discrepancy between measurement and simulation is from this non-perfect transistor noise model along with the noise in the control line and power supply that have not been included in the simulations.
The figure of merit ($FOM$) defined in [6] has been used widely to compare the performance of VCOs, but it doesn’t include the impact of the frequency tuning range. Recently a new figure of merit ($FOM_T$) including the frequency tuning range has been presented in [7]. Both $FOM$ and $FOM_T$ have been used to compare our design with other VCOs. The results of this comparison with other VCOs working around 20 GHz is shown in Table 1. Among the circuits that have been compared, this work shows the highest $FOM$ and $FOM_T$, and supports the effectiveness claim of the proposed topology for low-power low-noise, high-frequency VCO design.

4. Summary and Conclusions

We initially analyzed the maximum attainable oscillation frequency of VCOs that utilizes the widely used cross-coupled negative-$g_m$ cell. This analysis showed that
the finite base/gate resistance of the transistor and the equivalent parasitic capacitance ($C_{eq}$) of a negative resistance cell limit the maximum attainable oscillation frequency. The following analysis on the integrated differential negative resistance cell using a capacitive degeneration technique proves that it has a much higher max-
minimum attainable oscillation frequency and a much smaller equivalent shunt capacitance as compared to the cross-coupled negative-$g_m$ cell. This makes the VCO using a capacitively degenerated negative resistance cell a good choice for high-frequency integrated oscillators working close to the process $f_T$. The small equivalent capacitance is also useful to increase the tuning range of the oscillators operating at relatively low frequencies. The example design of a 5.3 GHz VCO in 0.25 μm CMOS technology shows a wider tuning range than VCO using a cross-coupled negative-$g_m$ cell without compromising on phase noise or power consumption.

Unfortunately, the capacitive degeneration technique reduces the effective transconductance of the cell, and hence the effective negative resistance, $R_{Eq}$, that is generated. We presented an active capacitive degeneration topology that can alleviate this problem. It uses a cross-coupled transistor pair as a degeneration cell. The cross-coupled transistor pair contributes additional conductance, and allows for the negative resistance cell to maintain a high maximum attainable oscillation frequency and have better negative resistance characteristics in comparison to the

<table>
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<th>Reference</th>
<th>Technology</th>
<th>Tuning Range (%)</th>
<th>$f_0$ (GHz)</th>
<th>FOM</th>
<th>FOM$_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>SiGe</td>
<td>14.5</td>
<td>20</td>
<td>-163.0</td>
<td>-166.3</td>
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<tr>
<td>[9]</td>
<td>SiGe</td>
<td>3</td>
<td>20</td>
<td>-154.7</td>
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<tr>
<td>[10]</td>
<td>InP</td>
<td>36</td>
<td>21.5</td>
<td>-154.3</td>
<td>-165.4</td>
</tr>
<tr>
<td>This work</td>
<td>SiGe</td>
<td>25</td>
<td>20</td>
<td>-172.7</td>
<td>-180.6</td>
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</tbody>
</table>

Fig. 35. Locking range and phase noise measurement results.
simple capacitively degenerated cell. These properties combined with its small effective capacitance enables low-power low-noise high-frequency VCO implementations. A prototype design for a 20 GHz fully integrated LC VCO implementation in the IBM SiGe 0.25 μm BiCMOS technology was demonstrated. A comparison of the figure of merit to previously reported 20 GHz VCOs supports the effectiveness of the active capacitive degeneration topology.

Although the VCOs using a capacitively degenerated negative resistance cell has been around in discrete design, the study for its application for fully integrated differential VCOs are fairly recently. The work presented in this paper proves the effectiveness of the capacitive degeneration technique through analytical derivations, simulations and measurements. The desirable characteristics discussed in this paper make the capacitive degeneration technique a promising candidate for high-frequency integrated oscillators.

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References


27. C. Patrick Yue, S. Simon Wong, “On-Chip Spiral Inductors with Patterned Ground


