HIGH PERFORMANCE FRC ADCs WITH GAIN CALIBRATION

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Abstract

In this paper we introduce an offline digital calibration technique that allows the feed-forward residue compensation (FRC) architecture to provide a 70-Msps 15-bit converter with a final spurious-free dynamic range (SFDR) of over 100dB. We develop analytical expressions for the maximum accuracy that can result from this architecture. Simulations of the overall architecture including device mismatch and finite amplifier gain were used to validate the calibration technique.

1 Introduction

The current trend to move the majority of the signal processing from the analogue to the digital domain simplify many aspects of the system, but it increases the performance requirements for the analog-to-digital converters (ADCs). In this paper we focus on the design of a data converter for universal cellular base stations that can handle multiple protocols. The majority of the cellular standards occupy a 25MHz spectrum bandwidth and have stringent requirements on linearity due to the presence of both very large and very small signals [1, 2]. With the requirement for an anti-alias input filter, the converter must actually operate at something over 50-M samples/s. These requirements arise because modern and future wireless base stations digitize the entire RF signal band and use digital filters to separate the received signal into the different channels. This technique allows for the software programmability of the channel selection and standard dependent demodulation needed for modern multi-standard receivers. We focus on the design of a 70-Msps, 15 bit ADC with a SFDR of over 95 dB.

Feed forward residue compensation (FRC) architectures combine a Nyquist rate converter with an over sampled converter and reap benefits of both architectures. This architecture exploits the inherent linearity of single-bit oversampled converters to provide the MSBs, but uses an auxiliary pipelined Nyquist rate converter to reduce the over sampling ratio (OSR) needed to a factor of four. The FRC architecture inherently performs an auto-zero such that the only remaining error is the gain mismatch between the primary and the auxiliary converters.

The FRC architecture was initially introduced with a high OSR to extend the resolution of low-speed Nyquist rate converters [7]. The high OSR architecture did not require gain error correction, but was unable to operate at the required 70-Msps. There is a tradeoff between the OSR and the gain error accuracy requirements. The relatively small over sampling ratio makes the proposed FRC architecture more sensitive to gain error at the input of the auxiliary converter. Finite op-amp gain, settling time and capacitor matching in the primary converter contribute to this gain error. As will be shown later, the output value of the primary converter is not affected by the gain error, but the output of the auxiliary converter output is. These gain error properties in the primary converter will be exploited to develop a purely digital offline gain error correction technique.

The number of offline calibration cycles and the timing of these cycles are parameters that could differ from implementation to implementation. For the particular implementation in this paper, the gain error correction technique uses the first 16 conversion cycles after reset or power-on to perform a self-calibration sequence. Because each conversion cycle takes 14 ns (corresponding to a 70-Msps rate), the calibration sequence requires 224 ns. This calibration uses an imprecise DC offset value derived from the reference voltage. Once this self-calibration sequence is performed, the circuit automatically configures to start converting the analog input to the corrected digital output. The calibrated converter operates as a fully functional high-resolution converter after the calibration is performed.

A time-domain expression for the voltages at the end of $n$ clock periods in the first-order FRC architecture can be written as shown in Equation (1) [7]:

$$V_o(n) = \frac{C_1}{C_f} \sum_{i=0}^{n-1} V_i(i) - \frac{C_2}{C_f} V_r \sum_{i=0}^{n-1} D(o(i)) + V_o(0)$$  \hspace{1cm} (1)

Under the assumption that $V_r$ remains constant with respect to the sampling rate, Equation (1) can be rewritten as shown in Equation (2):

$$V_r = \frac{1}{n} \frac{C_1}{C_f} \sum_{i=0}^{n-1} D(o(i)) + \frac{C_1}{C_f} \frac{V_o(0) - V_o(n)}{n}$$  \hspace{1cm} (2)
This assumption on $V_{in}$ is made only to simplify the equation discussion. Also any inaccuarcy induced by assuming $V_{in}$ is constant would contribute only to increased quantization error in the primary converter. As discussed earlier the auxiliary converter measures the primary converter quantization error. Further more, all the simulations presented throughout this paper are performed using complex sinusoidal inputs including estimated $KTC$ noise. The fundamental input signal frequency used for the simulations is between 50% to 100% of the converter’s Nyquist rate. The Nyquist rate in the presented architecture and used in the simulations is 35 MHz. For further simplicity, normalizing $V_{ref}$ to one, setting all capacitors to equal values then Equation (2) can be simplified further as shown in Equation (3):

$$V_o = \frac{1}{n} \sum_{i=0}^{n-1} D_0(i) + V_o(0) - V_o(n)$$

(3)

Where $n$ is the number of primary converter clock cycles used for one sample during the conversion process, i.e., the OSR.

2.1 Intuitive Look at Gain Error

Before deriving detailed error correction equations the following intuitive look at the gain error effect is presented. The effect of the gain error is to reduce the accuracy in the auxiliary converter. The accuracy of the primary converter is not affected by gain error in the converter as can be observed by examination of Fig. 2 and will be shown in subsequent sections where the normalized gain is present only in auxiliary converter terms.

When there is a gain error in the system and after the calibration offset is introduced the output of the FRC oscillates as shown by the bold line in Fig 2.
gain error of less than one is present, the auxiliary converter estimates a value that is somewhat greater than the \(-0.25\) if the primary converter output is zero and a value that is somewhat smaller than the \(+0.25\) when the primary converter output is \(-0.5\). The reverse is seen when a normalized gain error of more than one is present. The amplitude of the ripple is directly proportional to the gain error. The gain error correction algorithm presented in this paper essentially consists of estimating this ripple and finding a post processing mechanism to minimize it.

### 2.2 Gain Error Correction Equations

The gain error correction method presented here uses only digital post processing. It requires only a small change to the converter allowing the analog design to be optimised for performance. The presented architecture requires the addition of a non-critical calibration offset and the stopping of the input’s sample and hold clock. The method presented was simulated using assuming a digital hardware implementation, but the algorithm could also be implemented in software and potentially on existing systems if a method to input the calibration offset exists. The calibration offset could be a potential on existing systems if a method to input the calibration offset exists. The calibration offset could be a

To develop the set of equations for the gain error, let ‘b’ represent the normalised gain including any error in the primary converter loop of the FRC architecture shown in Fig. 1. Starting with Equation (1) and again assuming \(V_{in}\) to be constant with respect to the sampling rate and adding the gain term we form Equation (4) shown below:

\[
V_0(n) = b C_1 C_2 \sum_{i=0}^{n-1} V_x(i) - b C_2 V_{ref} \sum_{i=0}^{n-1} D_0(i) + V_0(0)
\]

\[
b V_a = b \frac{1}{n} C_1 C_2 \sum_{i=0}^{n-1} D_0(i) + \frac{C_1 V_0(0) - V_0(n)}{n}
\]

\[
V_a = \frac{1}{n} C_1 C_2 \sum_{i=0}^{n-1} D_0(i) + \frac{1}{b} \frac{C_1 V_0(0) - V_0(n)}{n}
\]

Again for simplicity, we normalize \(V_{ref}\) to one, set all capacitors to be equal in value then Equation (4) can be simplified as shown in Equation (5):

\[
V_a = \frac{1}{n} \sum_{i=0}^{n-1} D_0(i) + \frac{1}{b} \frac{V_0(0) - V_0(n)}{n}
\]

Upon examining Equation (5) above, the first term is the result from the primary converter and the second term is estimated by the auxiliary converter. It can be seen that only the terms from the auxiliary converter have the ‘b’ gain term in them. As discussed earlier the gain error only affects the output of the auxiliary converter.

Now to develop an equation for the normalised gain term “b”, take the expression for \(V_{in}\) shown in equation (5) above for two consecutive samples and set them to be equal to each other. This is valid because during the time that “b” is calculated, \(V_{in}\) is a constant value equal to the calibration offset. The equation for estimating “b” can be written as shown in equation (6):

\[
b = \frac{\sum_{i=n}^{2n} D_0(i) - \sum_{i=2n}^{3n} D_0(i)}{\sum_{i=2n}^{3n} D_0(i)}
\]

Where

\[
\sum_{i=n}^{2n} D_0(i) = \frac{1}{n} \sum_{i=2n}^{3n} D_0(i)
\]

### 2.3 Gain Accuracy Requirement Equations

After the equation for the normalised gain “b” is developed, it is instructive to examine the worst case gain error to understand why gain error is so important in this architecture. The largest gain error effect occurs when the value of the auxiliary converter is at the maximum or minimum. This is just before the primary converter makes a step to the next value. The gain error is the maximum when the second term in Equation (5) is a maximum. When the number of bits in the primary converter is given by ‘x’ and the number of bits in the auxiliary converter is given by ‘y’ then Equation (7) provides the maximum error under these conditions.

\[
\max(V_0(n) - V_0(2n)) = \frac{1}{2^{(x+y)}} - \frac{1}{2^{(x+y)}} (0) = \frac{1}{2^x}
\]

\[
\frac{1}{2^{(x+y)}} \geq \frac{1}{n} \sum_{i=n}^{2n} D_0(i) + \frac{1}{b} \frac{1}{n^2}
\]

\[
1 + \frac{n}{2^y} \geq \frac{1}{b}
\]

This equation is developed by calculating the difference in Equation (5) with and without any loop gain error. The results should also be less than 1 LSB in magnitude. The gain error is also at a maximum when the second term in Equation (5) is a minimum. Once again, when the number of bits in the primary converter is given by ‘x’ and ‘y’ bits in the auxiliary converter Equation (8) provides the maximum error under these conditions.

\[
\min(V_0(n) - V_0(2n)) = \frac{1}{2^{(x+y)}} (0) - \frac{1}{2^{(x+y)}} (2^y) = -\frac{1}{2^y}
\]
The normalised gain term ‘b’ must simultaneously meet both conditions in Equations (7) and (8). This leads to the result shown in Equation (9).

\[
1 - \frac{n}{2^y} \leq \frac{1}{b} \leq 1 + \frac{n}{2^y} 
\]  

(9)

In the proposed architecture ‘n’ = 4 and ‘y’ = 13. This leads to a gain accuracy (capacitor matching requirement) of ±1/2^{11} or 0.05% which is close to the limit of what is possible using current technologies [12, 13, 14]. The capacitor matching limit restricts auxiliary pipeline ADC to 12-13 bits with an ratio-matching yield [13]. Additionally, capacitor matching is inversely proportional to capacitor area (i.e., size) which places limits on maximum operating frequencies. Therefore, if we are able to calibrate any gain error then we have the potential of using smaller capacitor sizes [15].

Upon examining Equation (9) above, one might conclude that the architecture should be changed to reduce the dependence on gain accuracy by increasing the over sampling ratio. To achieve the goal of 70-Msps the auxiliary converter is operating at a clock frequency of 70 MHz. This in turn requires the primary converter to operate at a 280 MHz clock with an UGF of 472 MHz. If the over sampling ratio was increased from 4 to 8, this would improve the capacitor matching issue but would require the primary converter to operate at 560 MHz with an UGF of 944 MHz. At these higher frequencies the finite gain and slew rate of the amplifier in the primary converter can become problematic. Even if the over sampling was increased to 8, the required gain error of less than 0.1% would be very difficult to achieve as it does not allow for any of the other smaller contributing factors like finite op-amp gain that contribute to the overall gain error. It would be expected that the lower over sampling ratio with the correction technique would also lead to increased device yield and reduced cost as the capacitor matching requirements are reduced.

### 3 Gain Error Correction Architecture

In Fig. 3, sections A, B and C are the same as the base FRC architecture shown in Fig. 1. The additional circuitry that is required for the gain error correction scheme presented can be determined by examining sections D, E and F. Section E performs the computation of the normalised gain term ‘b’ given by Equation (6). Section F averages the computed ‘b’ term over a number of samples to provide a more accurate result by reducing quantization error. The division on the output of section F applies the gain error correction estimate to the auxiliary convert’s output before it gets merged with the primary convert’s output to form the total FRC converter output.

The only change to the analog circuits is the addition of C_{co} and the controlling of switches shown in section D of Fig. 3. The ADC Control logic is also modified to stop switching C_{1} and switch C_{co} during the calibration cycles. C_{co} is used to generate the calibration offset and has the same capacitor matching limits as the overall converter. As stated earlier capacitor mismatch is the principle contributor to the gain error in the FRC data converter. It can be seen from Fig. 4 below that the architecture shows little effect from a variance of ±20% in the calibration offset and consequently is not sensitive to the accuracy of the calibration offset. This allows for less stringent circuit design requirements.

The FRC architecture is not sensitive to offset error in the primary converter as two consecutive samples from the auxiliary converter are subtracted from each other and any offset in both samples will cancel. Under practical design conditions offsets in the range of 5-10 mV will be present in the design and could be used for the calibration offset. The designer may design in a small constant offset on the circuit without affecting the circuit. But in the proposed design, we have designed a circuit to set the calibration offset at −0.25 of V_{ref}.

Lastly, the finite gain of the amplifier must also be investigated as it will contribute to the gain error and it will also shift the pole of the integrator away from the unit circle. As already mentioned, the dominate factor in the gain error is capacitor mismatch, but the shifting of the pole can be very problematic.

Fig. 5 below shows the effects of the integrator’s finite op-amp gain on the proposed architecture.
The simulations shown in Fig. 5 indicate an op-amp gain requirement of about 85 dB for a SFDR of 100 dB. The effects caused by finite amplifier gain can be reduced by gain squaring techniques [7, 16, 17]. As shown in Fig. 5 the op-amp gain requirements are reduced to about 43 dB when gain squaring is employed. The gain squaring technique does not require any additional circuit bandwidth or clock cycles.

If an op-amp is designed with 60 dB of gain and an UGF of 500 MHz it will meet all of the requirements for this proposed architecture. These requirements are easily achievable in today’s standard CMOS technology.

4 Simulation Results

Fig. 6 shown below is a plot of simulated power spectral density of the data converter output for an input frequency of 28 MHz with no gain error present. The second input tone is a low amplitude low frequency term added just to ensure adequate complexity of the input signal to make the simulations more realistic. It also behaves as a dither signal to reduce limit cycles that are present in low order sigma-delta converters. All simulations also include estimated KT/C noise of the sampling switches. This figure is provided as a reference to compare against the later simulation results. The maximum noise level is -122.7 dB, a signal amplitude is of -8.9 dB and a converter SFDR of 113.8 dB.

Fig. 7 shown above is a plot of simulation results with an input frequency of 28 MHz, the same as in Fig. 6, and a 0.1% gain error without the proposed gain error correction technique.

This is also provided as a reference to compare against the results in Fig. 8. The maximum noise level of this simulation is -84.8 dB, signal amplitude of -8.9 dB and a resulting SFDR of 75.9 dB. This is about a 38 dB reduction in the converter’s SFDR performance caused by only a 0.1% gain error.

Fig. 8 shows a plot of the simulation results with an input frequency of 28 MHz and a 0.1% gain error, the same as in Fig. 7, with the proposed gain error correction technique. These results are compared to Fig. 7. The maximum noise level of this simulation is -123.5 dB, signal amplitude of -8.9 dB and a SFDR of 114.6 dB, which is about a 39 dB improvement over the uncorrected results. The 0.8 dB discrepancy in the converter results without gain error, shown in Fig 6, and the results shown in Fig 8 is insignificant and is a result of the stochastic properties of noise.

To demonstrate the robustness of the proposed correction technique a series of simulations were performed at an input frequency of 0.8 FS and with a 1% offset calibration error while the gain error was varied. Fig 9 is a plot of the minimum SFDR for each of the 800 simulations.
The simulation results shown are for a gain error of ±4%. The simulation results in Fig. 9 shows good performance of the architecture over a wide range of gain errors. It is assumed that the actual gain error that needs to be corrected will be less than 1% as capacitor match can achieve an accuracy of about 0.1% - 0.05% \([12, 13, 14]\). The minimum SFDR of these simulations is 107.5 dB for a two-tone input at 700 KHz and 28 MHz. The second tone is dominant at 79% of the full-scale amplitude.

5 Conclusion

In this paper, a practical technique for gain error correction in a FRC architecture was shown. This technique allows the FRC architecture to be used to extend the bits of resolution of high performance state-of-the-art pipeline ADCs. We have developed expressions for the maximum accuracy, including component limitations, which can result from this architecture. The validity of the gain error correction technique has been validated by the use of MATLAB simulations. We have also shown that with the proposed gain error correction technique a practical FRC ADCs can achieve a SFDR of over 100 dB at a 70-Msps rate.

References


