High Speed Frequency Hopping Using Injection Locked Front-Ends

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Invited Paper

Abstract—Direct digital synthesis (DDS) systems allow for the generation of accurate and versatile analog waveforms. However, DDS’s have been limited in generating very high frequency signals. In this paper, we show that a combination of a DDS and harmonic injection locking can result in a very low power and area-efficient high-frequency synthesizer. We show that injection locked oscillators (ILOs) are capable of almost instantaneous locking and we also present the related understanding related of the frequency acquisition process in ILOs. We use this understanding to develop a new architecture for DDS operation. The novel architecture presented in this paper preserves the advantages of DDS such as very high speed frequency hopping and can generate RF frequencies which is not possible with traditional DDS circuits. Simulation results for a 7 GHz oscillator with fundamental and harmonic injection locking are used to validate the instantaneous locking necessary in a high frequency DDS.

I. INTRODUCTION

The rapid hopping between frequencies is extremely important in modern spread spectrum wireless communication systems. Spread spectrum systems provide excellent interference immunity and security. In particular, frequency-hopped spread spectrum (FHSS) systems rely on frequency diversity and fast frequency hopping to achieve these properties. Frequency settling of local oscillators within the specified guard band is critical in such systems. For example, the Multi-Band OFDM Alliance (MBOA) Ultra-Wide Band (UWB) specification imposes a 9.5 ns settling time on the frequency synthesizer. Traditional techniques using phase-locked loop (PLL) structures require prohibitively wide loop bandwidths to achieve such settling times. Direct digital synthesizers can be extremely agile but have traditionally been limited to lower frequencies.

In this paper, we propose a novel architecture for a high frequency direct digital synthesizer. We use a combination of a DDS and harmonic injection locking to achieve this. The locking time in injection locked oscillators shows a strong dependence on the initial phase difference between the injected signal and the oscillator signal. This forms the basis for the design. Section II presents the basics, advantages and limitations of direct digital synthesis. The new architecture and the relevant theory are presented in Section III. The proposed architecture is validated using simulations of fundamental and harmonic injection locking and the results are presented in Section IV. We close with a few conclusions in Section V.

II. DIRECT DIGITAL SYNTHESIS

Direct digital synthesis is a digital technique to generate accurate and versatile waveforms. The basic architecture of a DDS (Fig. 1) comprises of a phase accumulator, a phase-to-sine/cosine converter and a D/A converter (DAC). The basic operation is best explained in the case of sine-wave generation. The phase accumulator generates the phase information and since there is definite relation between phase and the amplitude of a sine wave, the phase-to-amplitude conversion is done using a ROM look-up table. The DAC converts the sampled sine wave into an analog waveform. The $M$-bit control word determines the DDS output frequency given in (1).

$$f_{\text{out}} = M \times \Delta f \quad \Delta f = \frac{f_{\text{ref}}}{2^N} \quad (1)$$

where $N$ is the length in bits of the phase accumulator and $\Delta f$ is the frequency resolution of the DDS. Direct digital synthesis systems have a number of distinct advantages over PLL-based synthesizers.

- Complete digital control
- Very high frequency resolution and sub-degree phase resolution

![Fig. 1: Basic architecture for a direct digital synthesizer](image)
• Extremely fast hopping capability. The frequency hop can be made phase continuous; therefore there is no settling time associated with it.
• Excellent matching in polyphase synthesis (e.g., I and Q matching in quadrature generation).

The advantages of the DDS are more apparent if a modulated source is required. By choosing between different control words, the required modulation (i.e., frequency-shift-keying (FSK) or phase-shift-keying (PSK)) can be achieved. Fig. 2 shows a potential scheme to generate a binary FSK (BFSK) signal. Since both control words are available, switching between frequencies can be very fast.

The primary disadvantage of the DDS comes from the fact that it essentially performs a division on the input reference frequency and the maximum operating frequency is limited to \( \leq \frac{f_{\text{ref}}}{2} \) (Nyquist theorem). The implementation of on-chip DACs [1] have allowed the use of higher reference frequencies and extended the operating frequency of the DDS but it is still limited to several hundreds of MHz or the lower GHz. This limits the applicability of DDS signal generators in wireless systems.

A. High frequency DDS

To increase the applicability of DDS, the frequency range needs to be extended. Using the DDS as a reference to a PLL is a straight-forward solution, but it has all the issues associated with analog PLLs. Alternately, up-conversion of the output from a low-frequency DDS, as in [2], using doublers and mixers can be used to generate wireless frequencies. An illustration is shown in Fig. 3. The additional circuitry consumes a lot of power and the multiplication leads to increased phase noise. Moreover, this is also a very narrow band design and the distinct advantage of DDS agility is lost. Another solution is to generate higher harmonics of the fundamental signal and filter the required harmonic using some form of passive bandpass filtering to get the desired output. The power consumption associated with this technique can be made to be very low but requires very high quality factor (Q) filters to suppress the other undesired harmonics of the fundamental. Unfortunately, a filter output settles in approximately Q cycles of an input step change. Therefore, obtaining both fast settling and good spur suppression is difficult to achieve using high Q filters.

III. PROPOSED ARCHITECTURE AND THEORY

In this section we describe the architecture for the HF-DDS that uses a combination of a DDS and harmonic injection locking to achieve this.

A. Fast Locking

Injection locking in oscillators is well-described by Adler’s non-linear differential equation (2), where \( \phi(t) \) represents the phase difference between the instantaneous oscillator signal and the injected signal, where \( \omega_L \) is the single-sided lock-range of the oscillator, \( \omega_0 \) is the free running oscillator frequency and \( \omega_{\text{inj}} \) is the injected frequency.

\[
\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{\text{inj}}) - \omega_L \sin(\phi(t))
\]  

(2)

An approximate expression for lock range (\( \omega_L \)) and final steady state phase difference between injected and locked oscillator signals (\( \phi_{ss} \)) are given by (3), where \( I_{\text{osc}} \) and \( I_{\text{inj}} \) are the amplitudes of the oscillator core current and the injected current [3], [4].

\[
\omega_L = \frac{\omega_0}{2Q} \frac{I_{\text{inj}}}{I_{\text{osc}}} \quad \phi_{ss} = \sin^{-1}\left( \frac{\omega_0 - \omega_{\text{inj}}}{\omega_L} \right)
\]  

(3)

A solution to Adler’s equation (2) gives the time evolution of the phase difference between the oscillator signal and the injected signal asymptotically settling to \( \phi_{ss} \). The complete solution and the graphical interpretation are presented in [5], [6]. However, here we present only the small-signal linearized solution (4) to aid understanding.

\[
\phi(t) = \phi_{ss} + (\phi(0) - \phi_{ss}) e^{-\omega_L t}
\]  

(4)
From the linearized solution (4), it is evident that the lock time depends on the lock range \((\omega_L)\). As the lock range increases, the lock time becomes shorter. Fig. 4 illustrates the dependence of lock time on another critical parameter - the initial phase of injection, \(\phi(0)\). The plot shows that when the initial phase of injection, \(\phi(0)\), is equal to \(\phi_{ss}\), the locking is instantaneous. This is true even for small lock ranges. This can be explained by recalling that \(\phi_{ss}\) is the phase where \(d\phi(t)/dt = 0\). If the initial phase difference was exactly at \(\phi_{ss}\), it would remain at \(\phi_{ss}\). Moreover, the frequency of the oscillator would instantaneously jump from \(\omega_0\) to \(\omega_{inj}\) at \(t = 0^+\). Instantaneous locking is also evident from the linearized solution shown in (4).

**B. Proposed Architecture**

The proposed architecture is based on a low frequency DDS and harmonic injection locking of a digitally controlled oscillator (DCO). The block diagram is shown in Fig. 5. An injection locked oscillator behaves like a first-order PLL and generates the required high frequency output by locking onto a harmonic of the injected (reference) signal. The DDS core can be programmed to generate multi-tone signals, the simplest of which is a square wave. The digital controlled oscillator (DCO) is digitally tuned close to the required harmonic of the multi-tone signal. If sufficient signal power exists at the harmonic, injection locking occurs. A proper choice of the digital word from the DDS core controls the intrinsic frequency of the DCO. A DCO with a wide tuning range [7], [8] can be used to lock onto several harmonics of a low-frequency DDS signal, thereby making the overall design fairly wide-band. This is illustrated in Fig. 4.

The critical constraint on this architecture is to retain the agility of the DDS. The lock time of the ILO is therefore the bottleneck that decides the agility of the entire circuit. In this architecture, the lock time is minimized by exploiting its phase dependence. Consider the case where a DCO with free running frequency \(\omega_{01}\) is locked on to \(\omega_{inj1}\) and is abruptly switched to \(\omega_{02}\) to lock onto \(\omega_{inj2}\). The corresponding steady state phase are given by (5) where \(\omega_{L1}\) and \(\omega_{L2}\) are the respective lock ranges. Since the DCO is locked onto the DDS signal, at the instance of the switch, \(\phi_{ss1}\) becomes the initial phase of injection, \(\phi(0)\), for the next frequency. If \(\phi_{ss2}\) can be made close to \(\phi_{ss1}\) almost instantaneous locking is achieved. Also, since there is little phase settling, the frequency switch is nearly phase continuous. This can be accomplished by a proper choice of \(\omega_{02}\) such that \(\frac{\omega_{02} - \omega_{inj2}}{\omega_{L2}} \approx \frac{\omega_{01} - \omega_{inj1}}{\omega_{L1}}\). The two ratios may not be exactly equal, but if one can remain in the fast lock regions (marked by triangles in Fig. 4), the lock times are very small for all practical purposes. This is repeatable from one locked frequency to another except at the startup when the initial phase difference between the signals is not known.

One issue with ILO based high-frequency direct digital synthesis is the lack of variable amplitude. The amplitude control block, shown in Fig. 5 adds this feature to the architecture.

\[
\phi_{ss1} = \sin^{-1}\left(\frac{\omega_{01} - \omega_{inj1}}{\omega_{L1}}\right) \quad \phi_{ss2} = \sin^{-1}\left(\frac{\omega_{02} - \omega_{inj2}}{\omega_{L2}}\right)
\]

(5)
IV. SIMULATION RESULTS

In this section, we present simulation results to demonstrate the capabilities of injection locking based high frequency DDS. Shown in Fig. 7 is a PMOS-only oscillator with a parallel RLC tank. Switched capacitors are used to digitally control the frequency of the oscillator. $I_{inj}$ sources represent current injection to the oscillator. They can be single or multi-tone signals. As noted earlier, the versatility of the DDS is clearly evident when used as a modulation source. Here we use frequency shift keying (FSK) as the modulation scheme.

A. Fundamental FSK

Table I shows the circuit parameters and simulation conditions used for fundamental FSK - when the frequency of the DCO is close to the injected FSK signal frequencies. The injected signal is a single tone signal switching between low frequency and high frequency. The center frequencies of the DCO are chosen such that the resulting $\phi_{ss}$ are 12.48° and 13.0°. The frequency-settling behavior is plotted in Fig. 8(a). Long transient simulations were run and the period-to-period frequency was calculated from the zero crossings of the time domain data. The plot shows three curves: instantaneous frequencies of the free running DCO, the injected signal and the DCO under locking. At startup, the DCO oscillates at its center frequency. Since the phase difference between the injected and the oscillator signal is arbitrary, there is an exponential settling to the locked frequency. The settling time is dictated by both the lock range and initial phase [5], [6]. In this case settling occurs well before the first transition. Fig. 8(b) shows the transition from high to low frequency. The locked oscillator signal very closely follows the injected signal. Since each data point on the curve represents one period of the signal, the graph demonstrates that the locking occurs within two periods.

B. Harmonic FSK

The multiplication capability of the architecture is demonstrated using harmonic FSK. Here the DCO is tuned close to the seventh harmonic of a square wave injected signal. Any variation in the DCO frequency due to process or temperature can be calibrated out prior to final use [6]. The circuit parameters and simulation conditions used for harmonic FSK are shown in Table II. The square wave frequency was switched between 1 GHz and 1.021 GHz (corresponding to seventh-harmonic frequencies of 7 GHz and 7.147 GHz). The choice of center frequencies of the DCO resulted in $\phi_{ss}$ values of 25.8° and 26.8°, respectively. The simulation results are plotted in Fig. 9. The instantaneous frequency variation (blue) and the time-averaged frequency (red) is shown in Fig. 9(a). The time-averaged frequencies are very close to 7 GHz and 7.147 GHz. The magnified version, however, shows the periodic variation of instantaneous frequency with time which indicates the presence of other harmonics of the injected square-wave. The power spectral density (PSD) plot of the output signal in Fig. 9(b) further validates this conjecture. The two most significant spurs are at least 34 dB below the principal harmonic. However, their presence affects our technique for measuring the near instantaneous frequency by using zero-crossing periods. The frequency-switching capability shows that the output signal is able to switch in frequency nearly instantaneously.

V. CONCLUSIONS

This paper describes a novel HF-DDS system based on injection-locking. It provides an overview of the theory of the transient behavior of injection locked oscillators. The fast-switching capability and feasibility of the

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<th>Low frequency</th>
<th>High frequency</th>
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<tbody>
<tr>
<td>Center frequency ($f_0$)</td>
<td>7170 MHz</td>
<td>7165 MHz</td>
</tr>
<tr>
<td>Tank Q</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Injected frequency ($f_{inj}$)</td>
<td>7000 MHz</td>
<td>7147 MHz</td>
</tr>
<tr>
<td>Injection level ($I_{inj}/I_{osc}$)</td>
<td>0.133</td>
<td>0.133</td>
</tr>
<tr>
<td>Lock range estimate ($f_L$)</td>
<td>78.6 MHz</td>
<td>80.3 MHz</td>
</tr>
<tr>
<td>Steady state phase ($\phi_{ss}$)</td>
<td>12.48°</td>
<td>13.0°</td>
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TABLE I: Circuit / simulation parameters used for fundamental FSK
TABLE II: Circuit / simulation parameters used for Harmonic FSK

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<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Injected frequency ($f_{inj}$)</td>
<td>1000 MHz</td>
<td>1021 MHz</td>
</tr>
<tr>
<td>Injection level ($I_{inj}/I_{osc}$)</td>
<td>0.07</td>
<td>0.07</td>
</tr>
<tr>
<td>Lock range estimate ($f_L$)</td>
<td>39.0 MHz</td>
<td>39.9 MHz</td>
</tr>
<tr>
<td>Steady state phase ($\phi_{ss}$)</td>
<td>25.8°</td>
<td>26.82°</td>
</tr>
</tbody>
</table>

proposed HF-DDS architecture is demonstrated through high-frequency FSK simulations. The extremely fast-locking time requires accurate DCO frequency control. By careful design, the frequency hopping can be made phase-continuous. This technique provides all the advantages of the ILOs over analog PLLs such as lower power consumption and shorter settling time. In this paper we only provided details for FSK, however, it can be shown that any single carrier modulation would follow the same format of maintaining near zero $\phi_{ss}$ immediately before and after signal modulation. Slight modifications of the basic architecture are required to extend the technique to accommodate multi-carrier modulation formats.

**REFERENCES**


