Modeling and Synthesis of Wide-Band Switched-Resonators for VCOs

Bodhisatwa Sadhu, Umaikhe E. Omole, and Ramesh Harjani
University of Minnesota

Abstract—A two-level switched resonator model for synthesizing a wide-tuning range LC VCO is described. Viable resonator design styles are selected for achieving broadband frequency synthesis. A simple, generalized model is developed for design space exploration. Using this model, based on the performance specifications, a resonator style is selected. Also, the performance specifications are translated to individual component resonator components. At the second level, detailed models for the resonator components are developed. The resonator is then designed and simulated based on these models. As an example, a wideband VCO using a new inductor switching technique is explored. Simulations performed in a 0.18 µm CMOS process achieved a tuning range from 3.35 to 8.34 GHz while exhibiting phase noise between -107 and -119 dBc/Hz at 1 MHz offset over the entire range. The VCO core dissipated 1.9 to 8.3 mW power using a 1.8-V supply.

I. INTRODUCTION

The increased congestion of the wireless spectrum has made cognitive programmable radios highly desirable. To be able to operate over a wide range of frequencies, such programmable radios require very wide tuning range VCOs. Additionally, modern multi-carrier modulation schemes such as OFDM impose stringent phase noise specifications. In this paper we develop a two-level switched resonator model for synthesizing low phase noise, wide tuning range VCOs. The phase noise requirements make LC resonators the preferred choice. However, LC VCOs have traditionally been targeted for narrowband applications. Though switched inductor resonators provide a viable solution, very limited literature is available on the analysis and modeling of such systems. Therefore, the technique remains ill-exploited.

The general model developed in this paper provides design insight into the trade-offs involved in switched resonator circuits. More detailed models are then developed for circuit-level simulation. A method to synthesize wide-band, low phase noise LC VCOs based on these models is demonstrated.

The paper is organized as follows. In Section II, viable LC resonator styles for wideband VCO solutions are discussed. In Section III, generalized switched resonator model is developed and analyzed. Based on this model, a procedure for performing topology selection and translating the block-performance specifications into individual component specifications is developed. Detailed component modeling is then described in Section IV, and a design methodology for an optimized resonator based on these models is summarized in Section V. Simulation results from an example design used to validate the modeling and design framework are discussed in Section VI.

II. LC RESONATOR STYLES FOR WIDE-TUNING RANGE

LC VCOs can be tuned by changing the inductance, the capacitance or both [1]. In the absence of an effective method to continuously tune the inductor, the inductance value can be altered by switching to a new inductor [1], or by tapping a portion of a single inductor [2][3]. The first technique is area inefficient and is not considered in this paper. Capacitors can be varied stepwise by using switched capacitor banks, and continuously using varactors. A general model for a switched resonator is shown in Fig. 1.

III. A SIMPLE MODEL FOR DESIGN SPACE EXPLORATION

A simple model for the switched resonator is shown in Fig. 3. Only one inductor switch is analyzed here, though the analysis can easily be extended to multiple switches. The frequency of oscillation is given by \( f = \frac{1}{2\pi\sqrt{L_C}} \).

The two frequency banks obtained from the one switch inductor is shown in Fig. 2.

Here \( L_{\text{on}} \) and \( L_{\text{off}} \) are the effective inductances when the switch is on and off respectively, and \( C_{\text{min}} \) and \( C_{\text{max}} \) are the minimum and maximum capacitances attainable. We also define a switching ratio \( k = L_{\text{off}}/L_{\text{on}} \) where \( L_{\text{off}} \) is the fraction of the inductor switched out. In the ideal case, \( L_{\text{off}} = L_{\text{tot}} - L_{\text{on}} \). In order to obtain a continuous frequency range, we will make these frequency bands contiguous.

Without loss of generality, we assume that the switch is implemented by an nMOS transistor. We begin with simple models for the switch, depending on its region of operation. When on (transistor in triode), we can model the switch as a resistor in parallel with the switched out part of the inductor (Fig. 6). When off, it can be modeled (Fig. 4) as a capacitor \( C_{\text{off}} \) in parallel with the switched out part of the inductor (Fig. 6).

Using parallel to series transformations, we can absorb the switch parasitic into the inductor branch. An equivalent parallel RLC tank can then be constructed using series to parallel transformation of the combined inductor
branch parasitics (Fig. 4. to Fig. 8). As is evident, the inductor switch introduces parasitics that impact the performance. This comes as a price paid for the wider frequency range obtained, and as we will see, the technique is not beneficial for narrowband tuning.

IV. DESIGN INSIGHT AND RESONATOR SYNTHESIS

Based on the simple model developed, we now present a design example to illustrate quantitatively the trade-offs involved in switched resonator design. In the model described, the inductor and capacitor designs, switch size, and the switching ratio \( k \), are all design variables. The choice of inductors and capacitors for LC VCOs has already been explored in detail [4], and is fairly independent of the other variables. Given the finite length of this paper, and the mathematical clutter introduced by too many dimensions in our design space, we will focus only on choosing the switching ratio, and the switch size. For this example design, we use a frequency floor plan spanning 3-9 GHz, and a 1 nH spiral inductor based on criteria developed in [4] and will target the TSMC 0.18 µm technology.

From an exploration of the design space using this simple model, we will determine: 1) when switching the inductor is beneficial, and if so, 2) what is the optimal switching ratio \( k \), and 3) the optimal switch size.

We begin by deriving power and phase noise expressions based on this resonator model. Assuming a constant voltage swing at the output, the power dissipated can be derived as:

\[
\text{Power} = \frac{R_s V_d V_{sd}}{(aL)^2} \quad (1)
\]

Note that the worst case value occurs either at \( f_{\min} \) or \( f_{h_{\min}} \). As the inductance was chosen with due consideration to the power specification at \( f_{\min} \), we monitor \( f_{h_{\min}} \) for the worst case power performance. The power dissipation at \( f_{h_{\min}} \) is plotted Fig. 11.

Deriving the phase noise expression from Leeson’s model, we obtain:

\[
L(\Delta \omega) \equiv 10 \log \left[ \frac{kT_{F}}{V_{rms}} \left( \frac{\omega_0}{\Delta \omega} \right)^2 \right] \quad (2)
\]

Due to the \( \omega^2 \) term in expression (2), the worst case phase noise occurs at \( f_{h_{\max}} \). The phase noise at \( f_{h_{\max}} \) is plotted in Fig. 10. Observe that for resonators dominated by the inductor \( Q \), the phase noise reduces with a reduction in the effective series resistance, \( R_p \) (Fig. 7). Fig. 9 shows a plot of \( R_{mp} \) vs. \( k \) in the higher frequency bank. \( R_{mp} \) is lower than the effective parasitic resistance of an un-switched inductor \( (r=2.4 \Omega) \) only for higher values of \( k \). This provides a lower limit for \( k \) (condition 1) for obtaining phase noise benefit from switching.

The start-up condition for oscillation is given by: \( g_m R_p = (g_m L)/(C_p R_p) > 1 \). Interestingly, pure capacitive tuning by using a low inductance value violates this condition at some point, showing a basic limitation of capacitive tuning for broadband purposes. Even for the switched inductor resonator described here, this capacitive tuning limitation provides an upper bound for \( k \) (condition 2) if contiguous banks are desired.

Summarizing these two effects, from condition 1, switched inductor tuning is not beneficial for low \( k \) values where an alternative capacitive tuning solution is feasible (in narrowband applications). However, for broadband requirements, switched inductors not only provide a wideband solution where pure capacitive tuning fails (start-up condition), but also provides phase noise benefits as compared to pure capacitive tuning.

From Fig. 10 and Fig. 11, we note that the worst case power dissipation and phase noise increase drastically for high \( k \) values. These provide two more upper bounds for the value of \( k \) (conditions 3 and 4).

Also, from the plots in Fig. 9, Fig. 10 and Fig. 11, we note that the performance benefits from increasing the transistor width diminish beyond 600 µm. However, the parasitic capacitance continues to degrade linearly with increasing width, reducing the maximum frequency obtained. Based on this, we identify a 600 - 900 µm range for the optimum transistor width. Using this range, from the conditions 1, 3 and 4 derived, we find \( 0.25 < k < 0.65 \). Within these limits, we want to maximize \( k \) for a higher frequency range. We consider condition 3 later to ensure contiguous frequency banks.

V. DETAILED COMPONENT DESIGN

Using the simple analysis above, ranges for the switch size and switching ratio \( k \) were obtained. In this section, we will develop detailed models for the individual resonator components to capture and analyze several higher order effects. This will facilitate schematic level simulations and help complete and fine-tune the resonator design.

A. Switched Inductor Design And Modeling

The switched spiral inductor is shown in Fig. 12. Inductor tapping has been a recent research trend [2][3], and a detailed model of the switched on-chip inductor has not been developed. With the technique shown in Fig. 12, the relatively
low quality inner part of the inductor is switched out, as compared to previous designs [3]. The nMOS switch was carefully positioned to reduce the effect of its parasitics. Recall that the switch is within the substrate that is physically lower than the inductor coils.

A circuit model for the switched spiral inductor (Fig. 13) was developed in ADS. It is an extension of the frequency independent physical $2\pi\psi$ model proposed in [5]. The spiral is modeled as a distributed structure consisting of an inner $2\pi\psi$ network with series/ladder $RL$ elements $\{L_a, r_a, L_b, r_b\}$. These are nested within an outer $2\pi\psi$ network with series/ladder elements $\{L_s, r_s, L_c, r_c\}$. The inner section in Fig. 13 represents the portion of the spiral that has been switched out. A comparison of the simulated S-parameter components for the physical inductor (using Momentum) and the circuit model (using SpectreRF) shows excellent agreement over a wide frequency range (Fig. 14).

B. Switch Considerations

The trade-off between the switch on-resistance and off-capacitance was analyzed in the previous section. Here, we examine the frequency dependent substrate characteristics of the nMOS transistor in relation to the impact of the substrate response of the spiral. For this, the nMOS transistor model with resistive substrate network in [6] is converted via Y-transformation to an analogous model with frequency dependent shunt elements $R_{psub}$ and $C_{psub}$,

$$
R_{psub} = \frac{1}{(\omega C_{psub})^2 R_{sub}} + \frac{C_{psub}}{1 + (\omega R_{psub} C_{psub})^2}
$$

where $C_{psub} = C_{psub, off} + C_{psub, on}$ and $C_{psub} = C_{psub, off} + C_{psub, on}$ similar to the shunt elements of the inductor $\pi$-model of [7]. The shunt elements of the switch and the inductor are then compared for different switch widths. From an analysis of the increase in the parasitic interaction between the spiral and the switch with increasing switch size, and exact width is selected. For our example design, the switch is constructed using three $0.18 \mu m$ parallel MOS devices each with sixty-four $4 \mu m$ wide fingers (overall width of $768 \mu m$).

C. The Capacitance Bank

For this design, a capacitor bank was constructed using two 5-bit differential switched capacitor (using MIM capacitors) arrays, and pMOS inversion mode varactors. From simulations, the start-up condition was found to limit the frequency tuning range to only 3.1 GHz. For a higher tuning range, switching the inductor is necessary. In order to ensure contiguous bands, condition 2 needs to be satisfied. This limits the value of $k$ to $\sim 0.45$. Since this value is greater than that given by condition 1, we expect a lowering of the phase noise in the upper bank by using this technique.
VI. OVERALL DESIGN FLOW

The generalized design methodology developed and followed, based on the two-level model is summarized below.

![Flowchart summary of design methodology](image)

VI. SIMULATION RESULTS FOR A DESIGN EXAMPLE

A VCO was synthesized using the switched resonator flowchart above. Simulation results are discussed below. Table 1 gives a performance comparison of this design against recent work. The accurate modeling and optimized design strategy developed has helped us achieve an unprecedented wide tuning range (85%) with a good phase noise and reasonable power dissipation in simulation.

**Tuning:** Using the combination of discrete and continuous tuning described above, the VCO achieves a tuning range of 85%, from 3.35 to 8.34 GHz. The nominal VCO frequencies in the off and on switched inductor modes are 6.37 and 8.34 GHz. Considerable overlap of the frequency banks is ensured to account for process variations. The output voltage swing was kept approximately constant at 0.65V in the lower bank, and 0.5V in the upper bank (Fig. 15) by employing feed-forward current sources.

The power dissipation reduces with increasing frequency in each individual bank (Fig. 16) as predicted. The power dissipation varies from 1.9 mW to 8.3 mW.

The simulated phase noise is shown in Fig. 17. The plot does not show the predicted decrease in the phase noise when switching to the upper frequency bank due to a lower voltage swing here (0.5V compared to 0.65V in the low bank).

![Flowchart summary of design methodology](image)

### Table 1: VCO performance comparison

<table>
<thead>
<tr>
<th>Ref</th>
<th>f0(GHz)</th>
<th>Tuning Range (%)</th>
<th>Phase Noise (dBc/Hz)@1MHz</th>
<th>Power (mW)</th>
<th>CMOS (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>3.07-5.61</td>
<td>58.7</td>
<td>-114.6 to -120.8</td>
<td>2.0 - 3.0</td>
<td>0.13</td>
</tr>
<tr>
<td>[9]</td>
<td>3.37-8.34</td>
<td>85</td>
<td>-107 to -119.4</td>
<td>1.9 - 8.3</td>
<td>0.18</td>
</tr>
<tr>
<td>This work</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VI. CONCLUSION

A switched resonator has been modeled at two levels. Based on the high-level model, the number of switching segments, switch sizes and optimal switching points to meet particular specifications can be quickly obtained. The detailed model developed enable further design space exploration through circuit simulation, rather than protracted EM simulations. An example design based on this framework attains a tuning range of 85% with good phase noise and low power dissipation. The framework described fits the design of a variety of broadband LC VCOs, including multiple inductor switching topologies. An algorithm based on this framework is easily developed for automating the resonator design process.

REFERENCES