Exploiting the Transient Behavior of Injection Locked Oscillators

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Talk Outline

- Transient behavior of injection locked oscillators
  - Previous techniques for fast hopping
  - Transient theory
  - Framework verification
- Applications that exploit ILO transient behavior
  - #1: Fast hopping synthesizer
  - #2: Ultra-fast DDS
  - #3: Low power burst mode CDR
- Summary & acknowledgements
#1: MBOA UWB Synthesizer Requirements

- Multi-band OFDM UWB (3.1-10.6GHz, 528MHz channels)
- Requires < 9.5nS frequency hopping time

- Fast hopping issues for PLLs
  - Input crystal reference frequency limited to ~100MHz
  - Maximum loop bandwidth ~1/10 reference frequency
  - Too slow by about an order of magnitude

\[ T_{settling} \approx \frac{6}{\omega_n} \]

for 100MHz input reference and using 6

\[ T_{settling} \approx 96\text{ns} \]

Reference Input \( \rightarrow \) Loop Filter \( \rightarrow \) VCO

\( \omega_n \)

\( \div N \)

VCO output

9.5ns Guard Interval
Source: A. Batra, TI
Previous Architectures: Summary

- All the reported synthesizers
  - Use multiple PLLs
  - Use one or more stages of SSB mixing

- Issues with multiple PLLs
  - Increased power consumption
  - Inductor coupling and carrier leakage between PLLs

- Issues with SSB mixers
  - Increased power consumption
  - Phase and gain mismatches increase LO sidebands

- Spurious signals & LO sidebands
  - Reduces effective SNR & blocking
  - Hard to meet FCC transmit mask
New Architecture

- **Basic concept:** use harmonic injection locking
  - Injection locked VCO behaves like a 1st order PLL

- **Design characteristics**
  - Low frequency PLL for reference (264MHz)
  - Amplitude of Nth harmonic is < 1/N (equal to 1/N for square wave)
  - Low phase noise - clean “injected” signal
  - Low power, low noise

- **Wide band DCO**

- **Sub-harmonic injection locking**
  - 13th harmonic: 3432 MHz
  - 15th harmonic: 3960 MHz
  - 17th harmonic: 4488 MHz

![Diagram showing harmonic injection locking and frequency relations.](image)
Design constraints

- Static ILO properties well understood
  - Lock range, phase noise

- Other applications for ILOs
  - High-frequency division, quadrature generation
  - These applications place loose/no constraint on locking transient

- ILO behaves like a first-order PLL
  - Can ILOs be used for UWB frequency synthesis?

- For UWB application, ILOs should lock very fast (< 9.5 ns)
  - Need to understand their transient behavior
    - Dependence of lock-time on design parameters
    - Phase and frequency settling characteristics

- Spur suppression
  - Multi-tone injection
  - Adjacent channel spurs must be suppressed
Injection Locking of LC Oscillators

- For frequency $= \omega_0$, the phase through the tank is zero
- Let $I_{\text{inj}}$ be at $\omega_1$ and sufficiently large to injection lock oscillator
- For $\omega_1 < \omega_0$ the tank is more inductive $\Rightarrow$ V lead I
- $I_{\text{osc}}$ is in phase with $V_0$ (two negations)
- Barkhausen $\Rightarrow$ phase from $I_{\text{inj}}$ cancelled by tank at frequency $\omega_1$

$I_{\text{inj}} \ll I_{\text{osc}}$
Injection Locking: Phasors

- Low side injection (LSI) equivalent residual circuit (L’ << L)
- High side injection (HSI) equivalent residual circuit (C’ << C)
ILO: Phasors

- Assuming constant output voltage \( \Rightarrow I_{osc} \) is constant
  - I.e., voltage limited VCO design
- Low side injection

\[
\phi_{ss} = \phi_{inj} - \phi = \sin^{-1} \left[ \frac{(\omega_0 - \omega_{inj})}{\omega_L} \right]
\]

Case I

\[\begin{align*}
I_{osc} & \quad I_{inj} \\
\Psi_0 & \quad \phi_{ss}
\end{align*}\]

Case II

\[\begin{align*}
I_{osc} & \quad I_{inj} \\
\Psi_0 & \quad \phi_{ss}
\end{align*}\]

\[\omega_L \approx \frac{\omega_0}{2Q} \frac{I_{inj}}{I_{osc}}\]
Phase Trajectory: Stable & Meta-Stable

Adler’s equation

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \omega_L \sin[\phi(t)]$$

Graph showing the trajectory of \( \phi(t) \) over time with stable and meta-stable points indicated. The graph also differentiates between high side and low side injection.
Time Domain Solutions to Adler’s Equation

- Time domain solutions for phase & frequency trajectory

\[
\frac{d\phi(t)}{dt} = \left(\omega_0 - \omega_{inj}\right) - \omega_L \sin[\phi(t)]
\]

Phase trajectory

\[
\phi(t) = 2 \tan^{-1}\left[\frac{\omega_L}{\omega_0 - \omega_{inj}} - \frac{\omega_B}{\omega_0 - \omega_{inj}} \tanh\left(\frac{\omega_B (t - t_0)}{2}\right)\right] \quad \text{where} \quad \omega_B = \sqrt{\omega_L^2 - (\omega_0 - \omega_{inj})^2}
\]

Frequency trajectory

\[
\omega_{osc}(t) = \omega_{inj} - \frac{\omega_B^2}{\omega_0 - \omega_{inj}} \left[\text{sech}^2\left(\frac{\omega_B (t - t_0)}{2}\right)\right] - \frac{1}{\omega_B} \left[1 + \tan^2\left(\frac{\phi(t)}{2}\right)\right]
\]

Note: \(t_0\) is an integration constant and can be complex

Settling Time

\[
t = \frac{1}{\omega_B} \ln \left[\frac{\tan\left(\frac{\phi(t)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(t)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}\right]
\]

\[
t = \frac{1}{\omega_B} \ln \left[\frac{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}\right]
\]
Lock Time: Simplified Solution

- When both $\phi(0)$ and $\phi_{ss}$ are small
  - phase and frequency settling can be reduced to a more intuitive form

- Time constant for settling behavior proportional to lock range

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \omega_L \sin[\phi(t)] \approx (\omega_0 - \omega_{inj}) - \omega_L \phi(t)$$

$$\phi(t) = \phi_{ss} + \{\phi(0) - \phi_{ss}\} e^{-\omega_L t}$$

$$\omega_{osc}(t) = \omega_{inj} + \omega_L \{\phi(0) - \phi_{ss}\} e^{-\omega_L t}$$

- Injection locking time depends on lock frequency range
  - $4\tau$ settling $\Rightarrow 4/\omega_L$
  - For settling time $< 9.5$ ns (UWB spec) $\Rightarrow$ lock range $> 67$ MHz

- Is this feasible?
  - Center frequency : 3.5 GHz
  - $Q = 5$, $I_{inj} / I_{osc} = 0.2$
  - Results in a lock range $= 70$ MHz

Like 1st order RC / RL circuit
Phase & Frequency Settling: Model

- Solution to Adler’s equation ➔ phase and frequency trajectory
- Phase & frequency settling strongly depends on starting $\phi(0)$
- Phase asymptotically approaches $\phi_{ss}$ as $(t \to \infty)$
- Frequency changes abruptly at $t=0^+$ except when $\phi(0) \approx 0$ or $\pi$

![Graph showing phase difference and oscillator frequency over time](image)

- Phase Difference (rad)
- Oscillator Frequency (GHz)
- Time (ns)

Abrupt freq. change
Free Running freq.
Test Setups: Framework Validation

- **Simulation test setup**
  - PMOS transistor + grounded inductor + parallel resistor
  - Instantaneous frequency measured by considering zero crossings

- **Measurement test setup (I)**
  - Bipolar Colpitts oscillator
  - Time domain output measured by sampling scope (Agilent DSO 8104)
  - Instantaneous frequency measured by considering zero crossings

- **High freq ILO parameters**
  - Center freq: 3540 MHz
  - Tank Q: 5.8
  - $I_{\text{inj}}/I_{\text{osc}}$: 0.176
  - Estimated lock range: 52.75 MHz

- **Colpitts ILO parameters**
  - Center freq: 57.3 MHz
  - Measured lock range: 52.75 MHz
  - Theoretical worst lock time: 1.6μs
Frequency Settling: Model/Simulation/Measurement

- Current amplitude varies during locking depending on $\phi(0)$
  - Lock range varies with $\phi(0)$
- After 1st order correction
  - Good agreement with theory

Theory | Simulation | Theory corrected | Measurement

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Discrete Prototype Measurements: (57MHz)

- **Input frequency ramp**
  - Total frequency sweep: 8MHz
  - Near instantaneous frequency measured by zero crossings
  - Estimated lock range: 1.325 MHz

- **Slow beat / fast beat is a continuum**
Integrated Prototype Measurement Results 3.3GHz (I)

- Experiment 2: unlocked $\rightarrow$ locked
  - Achieved by ASK
- Frequency settling: from zero crossings
- Two lock ranges: 60 MHz and 100 MHz
  - Multiple readings recorded

- Lock range = 60 MHz
  - Best settling time: 8.2 ns
  - Worst settling time: 15.1 ns

- Lock range = 100 MHz
  - Best settling time: 4.1 ns
  - Worst settling time: 9.8 ns

EuMW '08

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Integrated Prototype Measurement Results 3.3GHz (II)

- **Experiment 1:** locked → locked
  - Achieved by FSK within lock range
- **Frequency settling:** from zero crossings
- **Two lock ranges:** 60 MHz and 100 MHz
  - Multiple readings recorded

<table>
<thead>
<tr>
<th>Experiment Set</th>
<th>Measured Lock Range</th>
<th>Estimated $I_{inj}/I_{osc}$</th>
<th>Injected Freq. I</th>
<th>Injected Freq. II</th>
<th>Measured Lock Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case I</td>
<td>60 MHz</td>
<td>0.21</td>
<td>Unlocked</td>
<td>3.36 GHz</td>
<td>Best: 8.23, Worst: 15.1, Average: 10.54</td>
</tr>
<tr>
<td>Case I</td>
<td>100 MHz</td>
<td>0.35</td>
<td>Unlocked</td>
<td>3.33 GHz</td>
<td>Best: 4.1, Worst: 9.8, Average: 8.23</td>
</tr>
<tr>
<td>Case II</td>
<td>60 MHz</td>
<td>0.21</td>
<td>3.45 GHz</td>
<td>3.34 GHz</td>
<td>Best: 2.66, Worst: 14.7, Average: 8.47</td>
</tr>
<tr>
<td>Case II</td>
<td>100 MHz</td>
<td>0.35</td>
<td>3.48 GHz</td>
<td>3.31 GHz</td>
<td>Best: 4.7, Worst: 10.02, Average: 6.85</td>
</tr>
</tbody>
</table>
Prototype Chip Architecture #1

- **Basic concept: use harmonic injection locking**
  - ILO behaves like a 1\textsuperscript{st} order PLL

- **Design characteristics**
  - Low frequency PLL for reference (264MHz)
  - Amplitude of Nth harmonic is < 1/N (for square wave)
  - Low phase noise - clean “injected” signal
    - VCO phase noise reduced/eliminated (depends on injection level)
    - Reference phase noise multiplied by N\textsuperscript{2} \leftrightarrow PLL
  - Low power (eliminated prescaler and high-frequency dividers)
  - Spurs arise from other odd harmonics of the square wave

- **Design tradeoff's**
  - Lock range and adjacent spur suppression

![Diagram](image)
Spur suppression is due to
- Regenerative amplification within lock range
- Injected signal amplified to the free running oscillator amplitude

**Simulated spur suppression**
- LC tank: $\omega_0 = 3.969$ GHz, $Q=6$
- Square wave current injection
- Un-equal high side and low side suppression

**Trade off between injection level and spur suppression**

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Injection Level</th>
<th>Suppression (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3432</td>
<td>$0.18I_{osc}$</td>
<td>5.1</td>
</tr>
<tr>
<td>3960</td>
<td>$0.12I_{osc}$</td>
<td>19.3</td>
</tr>
<tr>
<td>4488</td>
<td>$0.12I_{osc}$</td>
<td>29</td>
</tr>
</tbody>
</table>

- Passive LC tank
- $\text{linj} = 0.18 \times I_{osc}$
- $\text{linj} = 0.12 \times I_{osc}$
Spur Suppression: Linear Model

- The ILO can be modeled as a regenerative amplifier
- The transfer function for a passive RLC tank:
  \[ H(\omega) = \frac{A_0 \left( j\omega \frac{\omega_o}{Q} \right)}{\omega_o^2 + \left( j\omega \frac{\omega_o}{Q} \right)^2 + (j\omega)^2} \]
- With positive feedback:
  - Where \( \beta \) is very close to 1 (~0.999)
- Calculated spur suppression
  - \( \omega_o = 3.969 \text{ GHz}, Q=6 \)

\[ H_{fb}(\omega) = \frac{H(\omega)}{1 - \beta H(\omega)} \]

Passive LC tank
- \( \text{linj} = 0.18 \times \text{losc} \)
- \( \text{linj} = 0.12 \times \text{losc} \)

3432 MHz, 3960 MHz, 4488 MHz

5.1 dB, 19.6 dB, 23.1 dB, 18.5 dB, 21.9 dB
Spur Suppression (III)

- Simulation results
  - Circuit conditions: 3.396GHz, Tank Q=6
  - Two tone input signal
    - High side injection (@3.396 Ghz and 3.396 GHz + 528 MHz)

- Theory results
  - #1: Linear theory: from tank transfer function
  - #2: Non-linear theory
    - From Adler’s equation
    - Fourier expansion of phase modulation signal

![Graph showing suppression results](image)
ILO Spur Suppression: Measurements

- Two tone test (3.396GHz)
  - Equal amplitudes
  - Locking signal at the center of locking range
  - Injected spur @ +528MHz offset
Integrated Prototype Measurement 3.39GHz

- Measurement results integrated ILO
- Lock range
- 0.13μm CMOS
- Phase noise measurements

Different Injection Levels

W & W/O Lock

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#2: Direct Digital Synthesis: Introduction

- **DDS** is a digital technique
  - Frequency - tunable output
  - Phase - tunable output
- **Reference clock “divided down”**
- **Basic blocks**
  - Phase accumulator, phase \( \rightarrow \) amplitude, DAC, low pass filter
- **Frequency/phase controlled by digital input**
  - Digital word length determines resolution
- **Advantages**
  - Very high frequency/phase resolution
  - Wide tuning range
  - Excellent matching in polyphase synthesis
  - Ultrafast hopping times
- **Key limitations**
  - **Limited output frequency range**
    - Limited by max clock rate (fs/2) and DAC settling
  - Distortion / spectral purity

For RF applications \( \Rightarrow \) we need a **high frequency DDS**
High Frequency DDS: Some Techniques

- **DDS as a part of a PLL**
  - Frequency multiplication using a traditional PLL
  - Very high frequencies possible
  - Loses the agility advantages of a DDS

- **Up conversion**
  - Doubling/mixing can be used
  - Example: 2GHz DDS shown
  - Limited bandwidth
  - Loss of hopping capability

- **Passive band pass filtering**
  - Filter square wave harmonics
  - Low power consumption
  - Need high Q’s for spur suppression
  - Q cycles for settling (can be long)
High Frequency DDS: New Architecture

- Basic concept: use harmonic injection locking
  - Injection locked VCO behaves like a 1st order PLL
  - Near instantaneous locking

- Design characteristics
  - DDS core generates injection signal
  - “Square wave” input controls phase
  - Attenuator controls amplitude
  - Amplitude of Nth harmonic is $< 1/N$ (=1/N for square wave)
  - Low phase noise - clean “injected” signal
  - Low power, low noise

![Diagram of DDS architecture with reference frequency, DDS core, DCO, phase/freq control, and amplitude control. The output is tuned close to n*f₀.](image-url)
Settling Time: Instantaneous?

- **Settling equation**
  \[
  t = \frac{1}{\omega_B} \ln \left[ \frac{\tan \left( \frac{\phi(t)}{2} \right) - \cot \left( \frac{\phi_{ss}}{2} \right)}{\tan \left( \frac{\phi(t)}{2} \right) - \tan \left( \frac{\phi_{ss}}{2} \right)} \right] 
  \]

- **Tolerance of 0.1% assumed around stable settling values**

- **Settling is very fast if you are already there, i.e., \( \phi_{ss} \)**

- **Settling takes extremely long if near meta-stable point**

- **Low side injection**
  - \( \phi_{ss} \rightarrow \) stable
  - \( \pi - \phi_{ss} \rightarrow \) meta stable

- **High side injection**
  - \( \phi_{ss} \rightarrow \) stable
  - \( 3\pi - \phi_{ss} \rightarrow \) meta stable

![Graph showing lock time and initial phase of injection](image)
### Fundamental Injection (FSK)

<table>
<thead>
<tr>
<th></th>
<th>Low Freq</th>
<th>High Freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{\text{INJ}}$ (injected freq)</td>
<td>7.0 GHz</td>
<td>7.147 GHz</td>
</tr>
<tr>
<td>$F_0$ (osc free)</td>
<td>7.017 GHz</td>
<td>7.165 GHz</td>
</tr>
<tr>
<td>$F_L$ (lock range)</td>
<td>78.6 MHz</td>
<td>80.3 MHz</td>
</tr>
<tr>
<td>$\phi_{ss}$</td>
<td>12.48 (deg)</td>
<td>13 (deg)</td>
</tr>
</tbody>
</table>

$I_{\text{INJ}}/I_{\text{OSC}} = 0.133$

Tank Q = 6
# Harmonic Locking (FSK – 7th Harmonic)

<table>
<thead>
<tr>
<th></th>
<th>Initial</th>
<th>Final</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{\text{INJ}}$ (Injected freq)</td>
<td>1.0 GHz</td>
<td>1.021 GHz</td>
</tr>
<tr>
<td>$F_0$ (osc free)</td>
<td>7.017 GHz</td>
<td>7.165 GHz</td>
</tr>
<tr>
<td>$F_L$ (lock range)</td>
<td>78.6 MHz</td>
<td>80.3 MHz</td>
</tr>
<tr>
<td>$\phi_{ss}$</td>
<td>25.8 (deg)</td>
<td>26.8 (deg)</td>
</tr>
</tbody>
</table>

- $F_L$ = Locking onto $7 \times F_{\text{INJ}}$
- $I_{\text{INJ}}/I_{\text{OSC}} = 0.07$
- Estimated @ $7 \times F_{\text{INJ}}$

Ref: High Speed Frequency Hopping Using Injection Locked RF Front-ends, Asilomar 2007

Locked oscillator spurs

Tank $Q = 6$
#3: Burst Mode CDR

- Instantaneous locking required (eg: passive optical networks)
- Reference PLL used to track over PVT
- Cascade of injection locked VCOs used for constant output
- XOR-ing data and delayed version of data ➔ pulse slimming
- 20Gbps CDR in 90 nm technology
- Burst mode operation
  - Bit pattern preceded and followed by long runs of bits
- Instantaneous locking achieved (within 1 period, lock range 22MHz)
- ILO noise shaping improves phase noise performance
Low Power Burst Mode CDR With Sleep

- Example design
  - 5 GHz oscillator, Q=8, linj/losc ~ 0.5
  - Linear startup time \( \sim 1\)ns, locking time \( \frac{4}{\omega_L} \sim \frac{4}{1E9} = 4\) ns
  - Total time = 5 ns (10 clock cycles)

- For similar performance (PLL BW =200MHz, Ref Freq = 2GHz)

- Burst mode data (say 10 \% duty cycle in 100ns \( \rightarrow 10\)ns)

- Additional time needed for startup and settling 5ns

- Total on time of RX = 15ns \( \rightarrow \) RX can be shut down 85\% of time

---

![Diagram of data, CLK, ILO, and RX](image)

- Data
- CLK
- ILO
- RX

---

Data

CLK

ILO

RX

- OFF
- Startup & Lock
- Deskew
- OFF
- Startup & Lock
- Deskew

- ON
- OFF
- ON

---

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Talk Summary

- Developed understanding of transient & startup behavior of ILOs
- Described 3 applications that exploit this behavior
  - Fast hopping frequency synthesizer
  - Ultrafast DDS
  - Burse-mode CDR
- Injection locking been around for a long time but lots of new applications still being found
- Acknowledgements: students
  - N Lanka, S. Patnaik, KJ Sham, MR Ahmadi, B Sadhu, L Cai, M Sturm, J Kim, J Harvey, Shubba B
- Acknowledgements: financial support
  - SRC, Intel, DARPA, NIH, AME, UMC, LSI
- Related publications
  - Sub-10ns Frequency Hopping Synthesizer based on Injection-Locking, EuMW, 2008
  - Understanding the Transient Behavior of Injection Locked LC Oscillators, CICC 2007
  - Fast Hopping Injection Locked Frequency Generation for UWB, ICUWB 2007
  - High Speed Frequency Hopping Using Injection Locked RF Front-ends, Asilomar 2007