RF Outline

- Cognitive radio concepts
- Software defined radios
  - Mitola architecture
  - Data converter requirements
- Receiver considerations
  - Broadband approach
  - Channelization
  - Programmable narrowband approach
- Programmable Rx considerations
  - Wideband LNA
  - Wideband mixer
  - Wideband programmable VCO
- Programmable Tx considerations
- SDR summary
- Why CMOS & example SOC radios
Cognitive Radio: Spectrum Congestion

- Spectrum allocated to specific services
- Increased communications needs
  - From voice to data and video
  - Increased penetration of cell phones
  - Connected applications
- Solution: utilize all degrees of freedom
  - Space, Frequency, Time
- Dynamic spectrum access
- Spectrum underlay
  - Ultra-wideband communications
  - Min bandwidth > 500MHz
  - Signal level < -41dBm/MHz (part 15)
  - 3.1 GHz – 10.6 GHz band
- Spectrum overlay
  - Smart spectral usage
  - Opportunistically use underutilized bands
Cognitive Radio Frontends

- **Cognitive radio**
  - Proposed by J. Mitolla
  - **Software defined radio** + smarts
  - IEEE: A radio that can intelligently detect if a particular spectrum is available and jump to into/out of temporarily-unused spectrum very rapidly without interfering with the transmissions of other users (dynamic frequency access)

Determine location
Sense spectrum used by neighboring devices
Analyze and classify external environment
Changing frequency & bandwidth
Adjusting output power level
Alter transmission parameters & protocols

SDR or Programmable Wireless Radio

**FIGURE 1.** Spectral utilization during one day (50 MHz–1 GHz).
SDR Mitola Architecture

- Ideal SDR capabilities
  - Use any and all frequencies ($f_1 - f_2$) (e.g. $0.1GHz - 10GHz$)
  - User different modulation and access formats

- Moore’s law ➔ digital circuits faster and lower power
  - Do everything in digital
  - Need a sufficiently fast ADC & DAC with enough dynamic range
  - Seems like a good idea?

Mitola, Mitre Corporation, 1995
Receiver Considerations
Traditional Architecture: E.g. Zero-IF/Low-IF

- Suppress out of band signals using band select filter
- Channel selection (reject out of channel interferers)
  - Zero-IF: convert to DC, use LPF
  - Low-IF: converter to near DC, complex filter to suppress adjacent channel & other interferers, avoid offset and flicker
- Share dynamic range requirements between ADC and filtering
- Dynamic range requirements for ADC reduced significantly
  - E.g., WCDMA ➔ 9 bits, 200Msps ➔ power 3-4mW

*Low-IF architecture shown*
Filtering reduces dynamic range requirements for ADC.
Filtering Impact: GSM Example

- Blocking /interference specs for GSM

**FIGURE 2. Blocking Profile for GSM 900.**

J. Rudell, 1997
Dynamic Range Calculation

- **ADC noise distance**
  - Ensures ADC is not the top contributor

- **Signal-to-noise ratio (SNR)**
  - Required to achieve desired BER

- **Peak-to-average power ratio (PAPR)**
  - Choice of coding

- **Residual interference**
  - Most influential blocker
  - Attenuated by RF Filter / LNA / IF Filter

- **Headroom**
  - DC offsets
  - Gain errors in AGC
  - Transients
### Example Dynamic Range Calculations

<table>
<thead>
<tr>
<th>Specifications</th>
<th>GSM</th>
<th>WCDMA</th>
<th>UWB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Headroom (dB)</td>
<td>10</td>
<td>10</td>
<td>6</td>
</tr>
<tr>
<td>PAPR (dB)</td>
<td>3</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td>Residual interferers (dB)</td>
<td>45</td>
<td>20</td>
<td>5</td>
</tr>
<tr>
<td>SNR (dB)</td>
<td>10</td>
<td>-8</td>
<td>6</td>
</tr>
<tr>
<td>ADC distance (dB)</td>
<td>20</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>Required dynamic range (dB)</td>
<td>88</td>
<td>54</td>
<td>36</td>
</tr>
<tr>
<td>ENOB</td>
<td>14</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>Signal bandwidth (Hz)</td>
<td>200k</td>
<td>3.84M</td>
<td>528M</td>
</tr>
</tbody>
</table>

- Effective number of bits (ENOB) = \((SNR - 1.76)/6.02\)
- ADC noise distance 10dB ➔ 0.4dB degradation in SNR, 20dB ➔ 0.04dB degradation in SNR
Example Existing ADCs

<table>
<thead>
<tr>
<th></th>
<th>SNR (dB)</th>
<th>ENOB</th>
<th>Power (mW)</th>
<th>BW (MHz)</th>
<th>FOM (pJ/conv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>802.11b</td>
<td>60</td>
<td>10.0</td>
<td>20</td>
<td>44.0</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>10.8</td>
<td>60</td>
<td>40.0</td>
<td>0.8</td>
</tr>
<tr>
<td>Bluetooth</td>
<td>64</td>
<td>10.6</td>
<td>14.8</td>
<td>11.0</td>
<td>0.8</td>
</tr>
<tr>
<td>GSM</td>
<td>76</td>
<td>12.6</td>
<td>11.5</td>
<td>0.2</td>
<td>9.1</td>
</tr>
<tr>
<td></td>
<td>73</td>
<td>12.1</td>
<td>7.5</td>
<td>0.2</td>
<td>8.4</td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>15.0</td>
<td>3.8</td>
<td>0.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>82</td>
<td>13.6</td>
<td>10.5</td>
<td>0.2</td>
<td>4.2</td>
</tr>
<tr>
<td></td>
<td>83</td>
<td>13.8</td>
<td>8.3</td>
<td>0.1</td>
<td>5.9</td>
</tr>
<tr>
<td></td>
<td>83</td>
<td>13.8</td>
<td>8.3</td>
<td>0.1</td>
<td>5.9</td>
</tr>
<tr>
<td></td>
<td>71</td>
<td>11.9</td>
<td>1.65</td>
<td>0.2</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>77</td>
<td>12.8</td>
<td>12.7</td>
<td>0.2</td>
<td>9.0</td>
</tr>
<tr>
<td></td>
<td>84</td>
<td>14.0</td>
<td>5</td>
<td>0.2</td>
<td>1.6</td>
</tr>
<tr>
<td>WCDMA</td>
<td>53</td>
<td>8.8</td>
<td>13.5</td>
<td>3.8</td>
<td>7.9</td>
</tr>
<tr>
<td></td>
<td>83</td>
<td>13.8</td>
<td>4.1</td>
<td>1.2</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>76</td>
<td>12.6</td>
<td>28</td>
<td>2.0</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>12.5</td>
<td>17.8</td>
<td>2.0</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>12.5</td>
<td>17.8</td>
<td>2.0</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>46</td>
<td>7.6</td>
<td>2,945</td>
<td>1.9</td>
<td>7.9</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>10.3</td>
<td>127</td>
<td>3.8</td>
<td>26.3</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>12.0</td>
<td>3</td>
<td>2.0</td>
<td>0.4</td>
</tr>
</tbody>
</table>

- **FOM summary**
  - GSM: 0.6 pJ/conv
  - WCDMA: 0.24 pJ/conv
  - Bluetooth: 0.8 pJ/conv
  - 802.11b: 0.45 pJ/conv
  - ISSCC ’07: 0.065 pJ/conv

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FOM (pJ/conv)
Interferers: Blocking Signals

- Worst case RF measurements done around Bristol, England
- Strong signals: DCS1800 (-13dBm), TV (470-860MHz), GSM
- GSM sensitivity: -104dBm, 10dB carrier-to-cochannel interference
- With 6dB headroom ➔ 18bits

Watkins, 2003
Data Converter Figure of Merit (FOM)

- FOM for current day data converters
  - 0.2pJ/conv to about 1pJ/conv

\[
FOM = \frac{P}{2^{\text{SQNR}/6.02} (2 \cdot BW)} \quad \text{or} \quad \frac{P}{2^{\text{ENOB}} (2 \cdot BW)}
\]

<table>
<thead>
<tr>
<th>Signal Bandwidth (GHz)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>0.01</td>
<td>0.01</td>
</tr>
<tr>
<td>0.001</td>
<td>0.001</td>
</tr>
<tr>
<td>1.10^-4</td>
<td>1.10^-4</td>
</tr>
<tr>
<td>1.10^-5</td>
<td>1.10^-5</td>
</tr>
<tr>
<td>1.10^-6</td>
<td>1.10^-6</td>
</tr>
<tr>
<td>1.10^-7</td>
<td>1.10^-7</td>
</tr>
</tbody>
</table>

Using 0.19pJ/conv
Nyquist rate sampling

- 18bit, 5GHz $\Rightarrow$ 500W
- 18bit, 5GHz $\Rightarrow$ 9W
- Theoretical minimum limit
  KT/C + 1st stage amplifier
- 6bit, 5GHz $\Rightarrow$ 100mW

Typical cell battery 500mAh
@100W $\Rightarrow$ ~2 minute usage
SDR Approaches

- **Broadband approach**
  - Digitize the entire RF band of interest
  - Band & channel selection, demodulation done in digital domain
  - Highest flexibility
  - Power hungry approach
  - Most useful for military applications

- **Narrowband approach**
  - Only narrow band of RF frequencies of interest
  - Aka multi-standard RF frontends
  - But want complete flexibility in frequency and modulations
  - Programmable RF frontend

- **Intermediate approach**
  - Multiple non-contiguous narrow bands
  - Narrow band + broadband
SDR
Broadband Approach
Channelization: Time Interleaving

- Sophisticated digital signal processing can correct for path mismatch
- However, each ADC still sees the full bandwidth of the input signal
- Sample and hold design critical → jitter requirement severe
- Does not solve dynamic range issues

Typical 4 converter interleaved FFT
Channelization: Bandpass Filtering

- Uses the same # of ADC as time interleaving
- Reduced dynamic range requirement
- Sample and hold design still difficult (jitter still critical)
- High-Q bandpass filters not easily realizable

W. Namgoong, 2004
Bandpass Sampling: Jitter Requirements

- Bandpass sampling accomplishes both down conversion and sampling the signal
- White noise jitter model
  - Not completely correct if LO is generated by a PLL
  - But someplace to start & easy to understand

\[
X(t) = A_o e^{j\omega_o(t+\Delta t)} = A_o e^{j\omega_o t} e^{j\omega_o \Delta t} \\
\approx A_o e^{j\omega_o t} \left[1 + j\omega_o \Delta t \right]
\]

\[
\text{SNR} = \frac{A_o^2}{2\omega_o^2 \Delta t^2} = \frac{1}{\omega_o^2 \Delta t^2}
\]

\[
\Delta t_{\text{rms}}|_{\text{jammers}} = \frac{1}{2\pi f_{\text{max}} 2^N} \sqrt{\frac{2}{3} M}
\]

System Specs | Jitter
--- | ---
10GHz, 11bits, M=1 | 6fs

~1 to 2 orders lower than achievable

N = ADC resolution
M = oversampling

Thor & Akos, IEEE 2002

Figure 4. Frequency Domain Representation of Bandpass Sampling

Arkesteijn, Klumperink, Nauta, TCASII Feb 2006
Channelization: Lowpass Filtering

- Uses the same # of ADC as time interleaving
- Input bandwidth for each ADC reduced
- Easier sample and hold design
- More robust to sampling jitter but affected by LO phase noise
- Reduced dynamic range

W. Namgoong, 2004
Channelization: Calibration

- Channel equalization/calibration + AGC compensate for channel characteristics
- Maximum signal level limited due to AGC
- In single band approach all signal levels are lower due to blocker
- Here only one channel loses signal due to blocker
Channelization: Increased SNR

- DSSS UWB example
- 50dB narrowband interference
- For $b=4$ bit ADC, $M=5$ # of channels $\Rightarrow$ 20dB higher SNR
- Narrowband filtering helpful for low resolution ADCs

W. Namgoong, 2003
Receiver Circuit Blocks
Wideband LNA Design: Ladder Network

- Wideband, can have large interferers ➞ need high linearity
- Inductive source degeneration & ladder network input match
- Shunt peaked load
- NF~5dB, IIP3= -6.7dBm, $A_p=9.3$dB, 2.6-11.5GHz input match
- Power=9mW

Power Gain and Isolation

A. Belilacqua ISSCC 2004
Wideband LNA Design: Common Source

- Common-gate LNA with noise cancellation
  - Separate gain & input match considerations
- 0.13u CMOS, $A_p = 19\text{dB}$, IIP3=1dBm, NF~3-4dB, 0.5~6GHz

S. Chehrazi, CICC 2005
Wideband LNA Design: Resistive Feedback

- Use resistive feedback to perform impedance match
- Use increased input gm to reduce noise figure
- Inherently broadband, no inductors \( \Rightarrow \) small
- 90nm CMOS

Zhang & Taylor, ISSCC 2006
High-Linearity Mixer

- Wideband LNA ➔ potential for larger interferers
- Need extremely linear mixer, need higher IIP3 than LNA
- Passive mixers have highest linearity
- Harmonic rejection for improved LO harmonic rejection

Bagheri, ISSCC 2005
Channelized LO Design

- Require multiple LOs with finite spacing
- Good to be generated from same source → phase noise tracking
- Need to turn off for non-contiguous channels

Channelized Receiver LO Requirement

Potential Realization

A. Medi, IEEE SOC 2003
Receiver RF Power Breakdown

- Data for 100 mW GPS receiver
- 1/3 power consumed in PLL
  - Moderate phase noise
  - No channel switching
- > 1/3 power consumed in IF
  - Filters must be linear
  - High gain in IF (nonlinear)
- ¼ power consumed in RF
  - Narrow band, linear
- In many systems, ADC consumes additional power
- Digital processing consumption not included
- Atheros WLAN receiver
  - 250 mW Rx signal chain
  - 180 mW PLL
- PLLs are expensive (power)
- IF power increased due to linearity requirements
SDR
Narrowband Approach
### SDR Narrowband

- **Redefine SDR**
  - Receive 1 channel, any band, any channel bandwidth
  - No RF preselect filter
  - Selection accomplished by wideband LO + variable LPF

- **Example design**
  - Tune channel of interest to zero IF
  - Accommodate GSM (200kHz) and 802.11g (20MHz) (**100X**) | Bagheri, ISSCC 2005

---

**Full RX Chain Summary**

<table>
<thead>
<tr>
<th></th>
<th>GSM</th>
<th>802.11g</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF (High Gain) [dB]</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>IIP3 (Mid Gain) [dBm]</td>
<td>-3.5</td>
<td></td>
</tr>
<tr>
<td>IIP2 (Mid Gain) [dBm]</td>
<td>+65</td>
<td>+67</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>18-52</td>
<td>23-57</td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th></th>
<th>900MHz</th>
<th>5.3GHz</th>
</tr>
</thead>
</table>

---

**Active Area ~ 3.8mm²**
# Analog vs. Digital Signals

<table>
<thead>
<tr>
<th>Analog Signals</th>
<th>Digital Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous in amplitude</td>
<td>Discrete in amplitude</td>
</tr>
<tr>
<td>Continuous or <em>discrete</em> in time</td>
<td>Discrete in time</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Continuous Amplitude</th>
<th>Discrete Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Continuous Amplitude" /></td>
<td><img src="image2" alt="Discrete Amplitude" /></td>
</tr>
</tbody>
</table>

**Continuous Time**

**Discrete Time**

- SC Filters
- N bits
SDR Narrowband (II)

- Window integration sampler
- Time domain behavior

\[
y(t) \bigg|_{t=nT_s} = \int_{-\infty}^{\infty} x(\tau) w(\tau - nT_s) d\tau.
\]

- Frequency domain behavior

\[
|H(f)| = \frac{g_m T_s}{C} \left| \frac{\sin(\pi T_s f)}{\pi T_s f} \right|
\]

Figure 1. The first order WTS and its anti-aliasing pre-filter functionality.

First proposed by Carley & Mukerjee @1995 CICC
Lowpass Sampler w/ Internal Anti-Alias

\[ |H(f)| = \frac{g_m T_s}{C} \left| \sin \left( \pi T_s f \right) \right| \]

Rectangular Window Integration

- Main-lobe passes wanted signal at DC
- Side-lobes roll off with 20 dB/decade
- Notches @ \( n f_s \) for anti-aliasing
- Wider stop-band with higher \( f_s \)
Impulse Sampling vs. Integration Sampling

- Ideal impulse sampling
- Jittered impulse sampling

- You are essentially looking at the average over a $\Delta T$
- You are more susceptible to actual duration rather than absolute start and end times
- You also have the inbuilt anti-aliasing that comes with integration
Current Mode Sampling: Jitter (II)

- You are integrating over a period
- Variation of the sampling edge
  - Affects the depth of the null in the sinc
  - Introduces jitter in the aliased signal

\[
y_{\text{int}}(t) \approx \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) d\tau \\
+ \frac{1}{T_s} \left[ t_j(t)x(t) - t_j(t-T_s)x(t-T_s) \right] \quad (37)
\]

or, in terms of power spectral density, can be rewritten as

\[
S_{y_{\text{int}}}(f) = \left( \frac{\sin(\pi T_s f)}{\pi T_s f} \right)^2 S_x(f) \\
+ \frac{4}{T_s^2} (S_j(f) \ast S_x(f)) \sin^2(\pi T_s f). \quad (38)
\]

Mirzaei, TCASI, Nov 2008

Fig. 11. Reciprocal downconversion of the blocker due to clock jitter.
Sinc & Downsampling

- Initial sample rate may be very high, to protect the wanted channel
- A/D conversion at this rate wastes power, as wanted signal band is much lower
- Analog decimation filter? Yes ...

Ref: Abidi 2007

Lindfors, et al., 2003
Helsinki University
SDR Narrowband (III)

- Equal valued summation ➞ sinc filter

\[ Y(t) = \frac{1}{N} \sum x(t) \rightarrow \text{sinc} \]

- Triangle weighted summation ➞ sinc² filter
  - Convolution of two sinc functions

\[ (\cdot) = \frac{1}{N} \sum a_i x_i(t) \rightarrow \text{sinc}^2 \]
# Wideband VCO Design

- Combination of varactors & fixed caps
- Careful parasitic control
- Amplitude control for best phase noise

<table>
<thead>
<tr>
<th>Ref</th>
<th>Tech</th>
<th>Center Freq. (GHz)</th>
<th>Core Power (mW)</th>
<th>Tuning range</th>
<th>max $K_{vco}$ (MHz/V)</th>
<th>FOM (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>CMOS *</td>
<td>2.1</td>
<td>12.2</td>
<td>35%</td>
<td>330</td>
<td>+5.8</td>
</tr>
<tr>
<td>[2]</td>
<td>CMOS</td>
<td>2.6</td>
<td>10</td>
<td>26%</td>
<td>600</td>
<td>−3.1</td>
</tr>
<tr>
<td>[3]</td>
<td>SOI CMOS</td>
<td>4.33</td>
<td>2.0-3.0</td>
<td>58.7%</td>
<td>2250</td>
<td>+5.9-10.3</td>
</tr>
<tr>
<td>[4]</td>
<td>CMOS</td>
<td>1.8</td>
<td>32.4</td>
<td>28%</td>
<td>500</td>
<td>−3.8</td>
</tr>
<tr>
<td>[5]</td>
<td>CMOS</td>
<td>1.25</td>
<td>7.2</td>
<td>28%</td>
<td>70</td>
<td>−0.2</td>
</tr>
<tr>
<td>[6]</td>
<td>CMOS</td>
<td>2.12</td>
<td>10</td>
<td>30.5%</td>
<td>450</td>
<td>+1.9</td>
</tr>
<tr>
<td>[7]</td>
<td>CMOS *</td>
<td>2.1</td>
<td>2.0</td>
<td>28.6%</td>
<td>260</td>
<td>+5.7 **</td>
</tr>
<tr>
<td>[8]</td>
<td>SiGe BiCMOS</td>
<td>1.87</td>
<td>14-30.8</td>
<td>30%</td>
<td>45</td>
<td>+2-4</td>
</tr>
<tr>
<td>This work</td>
<td>CMOS</td>
<td>1.8</td>
<td>2.6-10</td>
<td>73%</td>
<td>270</td>
<td>+5.0-8.5</td>
</tr>
</tbody>
</table>

(* Uses bondwire for tank inductors, ** Best case)

Axel D. Berny et al. JSSC April 2005
Wideband VCO Design (II)

- Use a combination of mixers and frequency tuning

Yusaku Ito et al., ASSCC 2006
Wideband VCO Design (III)

- Traditional VCOs typically only switch capacitor to switch freq
  - Adding switch in series with inductor hurts phase noise
  - Inductors are physically large $\rightarrow$ multiple inductors $\rightarrow$ area

- For large tuning range with good phase noise
  - Switch both capacitors and inductors
  - But need to find a way to maintain tank Q

- Tank Q normally dominated by inductor Q

\[
\omega_o = \frac{1}{\sqrt{LC}}
\]

\[
Rp \approx Q_L^2 \cdot Rs = \omega_o^2 \frac{L^2}{Rs}
\]
Wideband VCO Design (III): Results

- U. Omole & Harjani 2007

Tank impedance

(a) $Z_{diff}$, lower band
(b) $Z_{diff}$, upper band
Wideband VCO Design (III): Results

### VCO Performance Comparison

<table>
<thead>
<tr>
<th>Ref</th>
<th>CMOS (µm)</th>
<th>$f_0$(GHz)</th>
<th>Tuning Range (%)</th>
<th>Phase Noise (dBc/Hz)@1MHz</th>
<th>Power (mW)</th>
<th>FOM (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>0.13 SOI</td>
<td>3.07-5.61</td>
<td>59</td>
<td>-114.6 to -120.8</td>
<td>2.0 - 3.0</td>
<td>5.9 – 10.3</td>
</tr>
<tr>
<td>[2]</td>
<td>0.18</td>
<td>1.8</td>
<td>73</td>
<td>-126.5</td>
<td>2.6 - 10</td>
<td>5 – 8.5</td>
</tr>
<tr>
<td>This work</td>
<td>0.18</td>
<td>3.37-8.34</td>
<td>85 (110)</td>
<td>-107 to -119.4</td>
<td>1.9 - 8.3</td>
<td>1.3 – 10.3</td>
</tr>
</tbody>
</table>


Ref: Sadhu & Harjani, CICC 2008
All Digital PLLs

**ADPLL motivation**
- Multiple radios on same chip ➔ small area
- Small feature size, lowered supply voltages
- Higher precision in time than in amplitude
- Minimize analog/RF circuitry

**Conventional PLL**
- Lots of analog circuits ➔ noise
- High KVCO in VCO ➔ phase noise
- Loop filter ➔ large, leaky, passive variations
- Difficult to calibrate, reference spurs
- Large lock times ~100us

**ADPLL**
- Time to digital converter
- Need to dither DCO
- Phase error is accumulated frequency error

B. Staszewski, CICC 2007, SMU 2006
All Digital Radios

- Old: RX use continuous time analog gain, mixing and filtering
- Not compatible with newer digital technologies
  - Lower amplitude precision (lower VDDs)
  - Higher time precision (higher $F_T$)
- $\rightarrow$ Sample data radios (not quite SDR)
  - Exploit digital processing
  - Exploit passive switched capacitor circuits
  - Integration in digital processes

Multi-radio integration
TI, Single chip GSM, 90nm CMOS

B. Staszewski, CICC 2007
Interference Suppression: RX

- Sophisticated digital techniques but requires large DR ADC
- Analog techniques before ADC more practical
- Feedforward narrowband active cancellation
  - Ranjit Gharpurey and Sahar Ayazian, IEEE DCSW, 2006
- Programmable passive filtering
  - B. E. Carey-Smith et.al., EURASIP J. on Wireless Com. & Networking, 2005

High-linearity, not lowest noise
Interference Suppression: RX Spatial

- Use beam forming (smart antenna) to place interferer in null

Taylor, VLSI 2007
Summary of SDR Talk

- **Cognitive radio concepts**
- **Software defined radios**
  - Receiver architecture & data converter requirements
  - Channelization & programmable frequency frontends
- **Circuit level issues**
  - Wideband LNA
  - Wideband programmable VCO
  - PA considerations
- **Other aspects not discussed**
  - Wideband antennas
  - Diplexer/circulator
  - Other RX considerations
    - LNA/mixer linearization
    - Programmable anti-alias filters
  - Other TX considerations
    - PA linearization, broadband techniques, power consumption etc.
    - DACs
  - MAC / BB / Software issues
- **Take away**
  - SDRs require a thorough understanding of system and circuit interactions
  - Cognitive radios require programmable wireless terminals as a platform
  - Interplay of software, architecture (RF + BB), and circuit make it extremely interesting
Why CMOS
&
CMOS Programmable Radio SOC Examples
Why CMOS?

- **Small footprint**
  - High-levels of integration
  - Integrate RF and DSP one chip
  - Multiple transceivers on-chip

- **Processing**
  - Significant amounts of DSP relatively free (1 inductor is ~ 100k gates)
  - Calibration: digitally correct analog imperfections
  - Significant memory capacity

- **Performance**
  - CMOS PAs demonstrated upto 2W
  - Ability to work at mm-wave
  - Timing (Multi-GHz clock rates)
  - High-level of frequency diversity

- **Cost**
  - Lower wafer costs than III-V (by about 10X, e.g., better yields)
  - Cheaper than discrete designs
    - Smaller boards, less components

Chip market ~$250B in 2008 SIA
Graphics from Soumyajit Mandal
Why CMOS (II)

- Technology

Ref: K. K. O et al., ISSCC’09

ITRS’08 Data & Projections for CMOS/BiCMOS
Why CMOS (III)

- Circuit designs

\[ F_{\text{min}} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_r} \sqrt{\gamma \delta (1 - |c|^2)} \]

Compiled from various publications in IEEE conferences/journals
### Example SOC Radios (I)

- Some single chip radios

<table>
<thead>
<tr>
<th>Institution</th>
<th>Reference</th>
<th>Technology (nm)</th>
<th>Area (mm²)</th>
<th>RF/analog area (mm²)</th>
<th>RF/analog supply (V)</th>
<th>TX architecture</th>
<th>RX architecture</th>
<th>LO architecture</th>
<th>TX current (mA)</th>
<th>RX current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atheros</td>
<td>ISSCC 06</td>
<td>180</td>
<td>33</td>
<td>12</td>
<td>3.0/1.8</td>
<td>Analog IQ</td>
<td>Analog IQ</td>
<td>ΣΔ CP-PLL</td>
<td>54</td>
<td>57</td>
</tr>
<tr>
<td>TI</td>
<td>ISSCC 08</td>
<td>90</td>
<td>24</td>
<td>3.8</td>
<td>1.5</td>
<td>Digital Polar</td>
<td>SC-IQ</td>
<td>ADPLL</td>
<td>47</td>
<td>56</td>
</tr>
<tr>
<td>Atheros</td>
<td>ISSCC 08</td>
<td>130</td>
<td>9.2</td>
<td>3</td>
<td>1.2</td>
<td>Analog Polar</td>
<td>Analog IQ</td>
<td>ΣΔ CP-PLL</td>
<td>19.3</td>
<td>29.7</td>
</tr>
<tr>
<td>Atheros</td>
<td>ISSCC 08</td>
<td>130</td>
<td>36</td>
<td>11</td>
<td>3.3/1.2</td>
<td>Analog Polar</td>
<td>Analog Polar</td>
<td>ΣΔ CP-PLL</td>
<td>280</td>
<td>310</td>
</tr>
</tbody>
</table>

B. Staszewski, ISSCC 09
Example SOC Radios (II)

- 2\textsuperscript{nd} generation TI DRP 90nm
- GSM cellular phone
- 1.2 billion phones sold 2007
- Continue growth emerging markets (need $20 phones)
- Extensive digital assistance

DRP is 16\% of Chip

B. Staszewski et al, ISSCC 08
Example SOC Radio (III)

- 130nm 36mm² WiLAN SOC
- 2x2 MIMO for 802.11n
- Calibration used extensively
  - RX dc offset
  - TX carrier leak
  - BB filter bandwidth
  - RX IQ mismatch
  - RX noise floor
  - ADC gain offset

Nathawad et al, ISSCC 08
Example Radio-Only (IV)

- Broadcom quadband GPRS/EDGE radio
- 130nm (die area = 8mm²)
- TX/RX power (254mA/140mA)

Darabi et al, ISSCC 08