A novel inductor switching technique is used to design and implement a wideband LC voltage controlled oscillator (VCO) in 0.13 μm CMOS. The VCO has a tuning range of 87.2% between 3.3 and 8.4 GHz with phase noise ranging from −122 to −117.2 dBc/Hz at 1 MHz offset. The power varies between 6.5 and 15.4 mW over the tuning range. This results in a Power-Frequency-Tuning Normalized figure of merit (PFTN) between 6.6 and 10.2 dB which is one of the best reported to date.

I. INTRODUCTION

With increasing congestion in the radio spectrum, multi-band multi-standard transceivers have gained prominence. These broadband systems require VCOs that achieve a wide tuning range coupled with stringent phase noise performance. Although LC VCOs are traditionally well-suited for low phase noise applications, their tuning range remains notoriously limited. For LC VCOs that employ only capacitance switching and/or tuning, the lowest achievable frequency is limited by the start-up criteria, and the highest achievable frequency is limited by the parasitic capacitance of the oscillator. Additionally, these systems are plagued by increased power at low frequencies and increased phase noise at high frequencies. As will be discussed in this paper, switching the inductance in addition to varying the capacitance eliminates these problems and provides a viable solution for obtaining very wide tuning ranges alongside low phase noise performance.

The paper is organized as follows. We discuss the advantages of inductance switching in Section II and describe a prototype design in Section III. We enumerate and discuss the experimental results in Section IV, and finally draw our conclusions in Section V.

II. TUNING OPTIONS IN LC TANK VCOs

Frequency variation in an LC tank can be realized by changing the capacitance and/or the inductance of the tank. Owing to a difficulty in the physical realization of high performance tuned inductors, pure inductive tuning is almost unknown. Capacitive tuning using varactors, or a combination of switched capacitors and varactors has been used frequently to obtain a wide tuning range. However, for a very wide-tuning range, pure capacitive tuning is not optimal. Instead the inductance may be switched [1]–[3] in order to provide separate frequency banks. Within these banks, frequency tuning may be accomplished through capacitive tuning. A detailed description regarding the tradeoffs associated with designing VCOs with inductor bands has been provided in [3] and is not provided here for space limitations.

A combined switching and tuning scheme, as described above, provides significant advantages over pure capacitive tuning for very wide tuning ranges. The reason can be explained through a simple comparison. Consider two different LC tanks: tank A where the frequency is tuned exclusively using capacitance variation, and tank B where the inductance is switched in addition to capacitive tuning.

For a constant voltage swing, the power dissipation of an LC tank VCO is given by equation (1), where \( R_s \) is the parasitic series resistance of the inductor and \( V_{sw} \) is the voltage swing.

\[
V_{sw} = \frac{(\omega L)^2 I_{bias}}{R_s} = \frac{(\omega L)^2 Power}{R_s V_{DD}}
\]

\[
\Rightarrow Power = \frac{R_s V_{sw} V_{DD}}{(\omega L)^2}
\]  (1)

Fig. 1 shows a plot of the power dissipation versus frequency for tanks A and B. As expressed in (1), the power dissipated for a constant voltage swing decreases with increasing frequency (slope of -2 on a log-log plot). Moreover, for tank A, Barkhausen's criteria determines the current at the lower frequencies causing a steeper decrease in power with increasing frequency (slope of -4 on a log-log plot).

However, in the case of tank B, since the power dissipated is inversely proportional to the inductance as expressed in (1), using a larger value of inductance in the lower frequency ranges causes a significant drop in power. Comparing the two tanks, the worst case power dissipation is significantly minimized in tank B as shown in Fig 1.

A similar observation can be drawn in the case of the phase noise of the VCO. From Leeson’s model, the approximate phase noise of the VCO is given by (2), which for \( \omega_0 \gg Q\Delta \omega \), reduces to (3). Here \( \Delta \omega \) is the frequency offset for the phase noise measurement, \( F \) is the noise factor, \( R_s \) is the parasitic series resistance of the inductor, \( P_{sig} \) is the signal power, \( \omega_0 \) is the oscillation frequency, and \( Q \) is the inductor’s

\[
\text{Phase Noise (dBc/Hz)} = 10 \log \left( \frac{1}{2 \pi F R_s Q^2} \right) + 10 \log \left( \frac{1}{2 \pi F} \right) + 10 \log \left( \frac{P_{sig}}{\omega_0^2} \right)
\]

\[
\Rightarrow \text{Phase Noise (dBc/Hz)} = 10 \log \left( \frac{1}{2 \pi F R_s Q^2} \right) + 10 \log \left( \frac{1}{2 \pi F} \right) + 10 \log \left( \frac{P_{sig}}{\omega_0^2} \right)
\]  (2)

\[
\Rightarrow \text{Phase Noise (dBc/Hz)} = 10 \log \left( \frac{1}{2 \pi F R_s Q^2} \right) + 10 \log \left( \frac{1}{2 \pi F} \right) + 10 \log \left( \frac{P_{sig}}{\omega_0^2} \right)
\]  (3)
Fig. 2. A comparison of phase noise between (a) tank A: an unswitched inductor resonator, and (b) tank B: a switched inductor resonator.

quality factor.

\[
L(\Delta \omega) = 10 \log \left\{ \frac{2FkT}{P_{\text{sig}}} \left( 1 + \frac{\omega_0^2}{2Q\Delta \omega} \right)^2 \right\} \tag{2}
\]

\[
\approx 10 \log \left( \frac{kTFR_s}{V_{\text{rms}}^2} \frac{\omega_0^2}{\Delta \omega} \right) \tag{3}
\]

Fig. 2 shows a plot of the phase noise versus frequency for tank A. As suggested by (3), the phase noise is seen to increase with frequency. In contrast, for tank B, the phase noise expressed in (3) is proportional to the parasitic series resistance of the tank, and for a tank dominated by the inductor quality factor, this parasitic resistance is proportional to the inductance to the first order. Therefore, phase noise decreases with a lowering of the inductance (lowering of the parasitic series resistance). Again, the worst case phase noise shows considerable improvement.

The improvement in phase noise by the introduction of a switch might seem counter-intuitive. Introducing a switch degrades the quality factor of an LC tank. However, as expressed in equation (3), the phase noise expression depends on the parasitic series resistance of the tank, rather than its quality factor. Therefore, as long as the parasitic resistance introduced by the switch is lower than the parasitic resistance of the inductor switched out, there is a net phase noise improvement due to the switching.

III. DETAILED DESIGN

Based on the inductor switching idea described above, we now present a complete prototype design as a proof of concept. For this design, we used a frequency floorplan spanning 3.3-8.3 GHz and targeted a CMOS only implementation in the IBM 130nm SiGe BiCMOS technology. For our particular application, since phase noise was an important criterion being considered, the cross-coupled nMOS pMOS topology in Fig. 3 was the appropriate choice.

For the design, an inductor switching scheme as proposed in [3] was used. An octagonal inductor with the switch positioned within and underneath it was designed as shown in Fig. 4. Based on the design methodology provided in [3], for a 1.2nH inductor, the switching ratio (\(k = L_{\text{off}}/L_{\text{tot}}\)) and switch width were determined to be 0.55 and 500\(\mu\)m respectively.

Within each frequency bank, the design was optimized based on the framework described in [4]. Special attention was paid to the layout of the VCO to ensure good tuning and phase noise performance. The effect of this is evident in the measurement results discussed later.

a) \(g_m\) cells: The \(W/L\) ratios of the \(g_m\) transistors were designed to allow a maximum current of 10mA. This allows start-up at the lowest frequencies of interest in the two bands, but causes the oscillator to function in the current limited regime (non-optimal phase noise as discussed in [4]). Such a design technique offers two advantages: it reduces the parasitic capacitance offered by the \(g_m\) transistors, and it limits the worst-case power dissipation of the VCO. Although this causes a degraded phase noise performance at the lowest frequencies, the lower frequencies do not determine the overall worst case phase noise over the entire tuning range (Fig. 2). Therefore, this degradation does not affect the overall phase noise performance of the VCO. In effect, the improved phase noise at the lowest frequencies is traded off for obtaining an improved power performance and tuning range.

b) Inductor: The inductor was designed as shown in Fig. 4. For the switching ratio obtained, the inductor switch had to be physically connected between the arms of the inductor’s inner coil. A very wide nMOS transistor (low resistance) was used as the switch, and was positioned directly beneath and within the inductor coil. As compared to placing the
switch outside the spiral, this reduces the effects of intercon-nect parasitics significantly. Higher order electromagnetic(EM) effects of placing the transistor beneath the inductor were considered [6], and the switch was placed away from the traces in order to reduce unpredictable capacitive coupling effects. Also, in this switching scheme, the relatively lower quality inner part [5] of the inductor is switched out, as compared to previous designs [2], thereby promising a better phase noise performance. The large switch size adds parasitic capacitance to the LC tank. However, by placing the switch close to the midpoint (small signal ground) of the differential inductor, the effect of these parasitics is considerably reduced. A high resistance substrate beneath the inductor in conjunction with a patterned ground shield are used to improve the quality factor of the inductor.

For the purpose of circuit simulations, an S-parameter 4-port network was used to mimic the switched inductor. For this, EM simulations were performed using ADS Momentum®, and the resultant S-parameter data was exported to Cadence Virtuoso® design environment for circuit simulations. In Cadence Virtuoso®, a rational interpolation scheme was used for periodic steady state analysis. This provided a simple and efficient way to include EM effects for the custom-made inductor in circuit simulations.

c) Capacitor bank: For the capacitor bank, a 5-bit, binary-weighted, differential, switched, MIM capacitor array was constructed for coarse frequency tuning. For fine frequency tuning, two differentially connected MOS varactors were utilized. The combination of discrete and continuous tuning ensures a desirable, lower value of $K_{VCO}$ for the oscillator. The switched capacitor array was constructed using multiple unit cells to provide good matching and ensure a monotonic frequency tuning characteristic.

IV. MEASUREMENT RESULTS

The design was implemented in CMOS in the IBM 130nm SiGe BiCMOS process. Fig. 5 shows a die photograph of the VCO. The total area including the bondpads is 0.87mm$^2$, and the area of the VCO core is 0.11mm$^2$.

Measurement results for the prototype design are discussed below. A table comparing the performance of this VCO with other recent publications is shown in Table I.

a) Tuning: For measuring the tuning range, the leakage output was coupled out by an off chip antenna to avoid the effect of loading from the 50Ω buffer and the probe pads. Using the combination of discrete and continuous tuning described above, the VCO achieves a frequency tuning range (FTR) of 87.2%, from 3.28–8.35 GHz at room temperature. The FTR increases with a decrease in temperature to 88.6% (3.28–8.52 GHz) at 0°C. As seen in Table I, the FTR obtained betters other previously reported wideband VCO solutions. When probed, the frequency tuning range reduces to 83.9%, from 3.2–7.82 GHz, due to the loading by a sub-optimally designed probe buffer, but is still better than prior designs.

Fig. 6 plots the frequency tuning of the VCO versus capacitor bank control voltages. Tuning in the low frequency band is shown using a + marked green line, and in the high frequency band using a * marked blue line. Note that all the binary weighted capacitors are not used for switching the frequency in the high frequency band. This is because, in the high band, the VCO fails the start-up condition for a lower capacitance as compared to that in the low frequency band.

The two frequency bands obtained by inductor switching achieve a 384MHz overlap as seen in Fig. 6. A considerable frequency overlap when switching capacitors is also ensured through the use of suitable varactors. This overdesign ensures a continuous frequency tuning in the face of process variations.

b) Power Dissipation: The power requirement of the VCO, as predicted for a constant voltage swing, reduces as frequency increases in each individual band (Fig. 7). The measured power dissipation for the core VCO varies from 6.6 to 14.1 mW in the upper band, and 6.5 to 15.4 mW in the lower band from a 1.6V supply. The trends expected in the variation of power dissipation with frequency are evident (compare with Fig. 1). The improvement in worst case power dissipation through inductor switching, as was promised in Section II, is obtained.

c) Phase Noise: For phase noise measurement, a buffer was included on chip in order to drive a 50Ω environment. The probed differential outputs were converted to a single-ended signal compatible with the measurement apparatus using an off-chip balun. Phase noise measurements were performed using an HP E4407B spectrum analyzer. A screenshot of the phase noise measurements at the lowest frequency point is shown in Fig. 8. The variation of the phase noise with the frequency (log scale) is shown in Fig. 9. The phase noise varies between $-122$ and $-117.5$ dBc/Hz at 1MHz offset in the lower frequency band, and $-119.6$ and $-117.2$ dBc/Hz.
at 1MHz offset in the higher frequency band. The trends expected in phase noise variation with frequency is evident (compare with Fig. 2). Again, an improvement in the worst case phase noise performance through inductor switching, as was promised in Section II, is obtained.

In order to evaluate and compare VCO performances, the Power-Frequency-Tuning Normalized figure of merit (PFTN) as described in [4] was used. A temperature of 300K was used for the PFTN calculations. Fig. 10 shows the VCO performance over the entire frequency range. The PFTN varies between 6.6 and 10.2 dB in the low frequency band, and 6.7 and 9.5 dB in the high frequency band. As shown in Table I, this design provides one of the best PFTN performances reported to date. Also notable is the lack of significant variation in the PFTN values over such a wide tuning bandwidth. This was ensured through a carefully designed trade-off between phase noise and power across the entire tuning range.

### TABLE I
VCO PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th>Ref</th>
<th>$f_0$ (GHz)</th>
<th>PFTN (%)</th>
<th>Phase Noise (dBc/Hz) @1MHz</th>
<th>PFTN (dB)</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>4.34</td>
<td>58.7</td>
<td>−120.8 to −114.6</td>
<td>5.9-10.3</td>
<td>0.13 SOI</td>
</tr>
<tr>
<td>[8]</td>
<td>1.8</td>
<td>73</td>
<td>−126.5 ($f_0$)</td>
<td>5.0-8.5</td>
<td>0.18 CMOS</td>
</tr>
<tr>
<td>[9]*</td>
<td>5.7</td>
<td>74</td>
<td>−104 to −101.5</td>
<td>−4.6-4.0</td>
<td>0.13 CMOS</td>
</tr>
<tr>
<td>This work</td>
<td>5.82</td>
<td>87.2</td>
<td>−122.0 to −117.2</td>
<td>6.6-10.2</td>
<td>0.13 CMOS</td>
</tr>
</tbody>
</table>

(*Simulation results)

V. CONCLUSIONS

In this paper, we explored inductor switching as a viable solution for obtaining very wide tuning range, low-phase noise LC oscillators. A prototype implementation using CMOS transistors was described that simultaneously achieved a phase noise between $-117.2$ dBc/Hz and $-122$ dBc/Hz at 1MHz frequency offset, and an unprecedented tuning range of 87.2% (or 83.9% with loading). The VCO core power varies between 6.5 and 15.4 mW from a 1.6V supply. This resulted in a PFTN that varies between 6.6 and 10.2 dB, which, to the best of our knowledge, is the highest reported to date.

REFERENCES