29.4 A Dual-Mode Architecture for a Phased-Array Receiver Based on Injection Locking in 0.13µm CMOS

Sathvik Patnaik, Narasimha Lanka, Ramesh Harjani
University of Minnesota, Minneapolis, MN

Phased arrays have long been used by the military for radar applications, but have only recently been applied to consumer applications. In a phased array system, one or more narrow beams are generated by transmitting (or receiving) a common RF signal that is phase shifted at the output of each antenna in the array such that the direction of the beams can be varied by controlling the phase difference between consecutive antennas. Microwave transceivers for phased-array radar applications have traditionally been fabricated in III-V technologies like GaAs and InP due to their superior fT and fmax. However, modern-day CMOS and BiCMOS technology nodes are now exhibiting fT and fmax in arithmetic progression, making the architecture an ideal candidate for today’s technology. Recent designs in CMOS have shown its capability to handle millimeter-wave frequencies [1-3].

This paper introduces two new phase-generation schemes, based on injection locking, for local oscillator (LO) phase-shifting phased-array receiver architectures. An integrated four-channel phased-array receiver operating at 2.4GHz is fabricated in a 0.13µm CMOS technology. The design consists of a mixer and a phase-generation oscillator for each channel, in addition to a four-channel intermediate-frequency (IF) summer and 256b serial register for digital programmability. This unique architecture exploits the steady-state phase at the output of an injection-locked oscillator (ILO) to create the desired phase-shift pattern. The four-channel receiver core draws only 42mW (10.5mW/channel) from a 1.5V power supply and occupies 1.2×1.2mm² of active area. This is approximately 50% lower power than phased-array receivers reported in the recent literature. The use of differential inductors can further improve the performance, and reduce the active area of the receiver.

Injection locking for phased-array radar has been used previously in [4], where weak coupling via the antennas was utilized for phase-shift generation. Weak coupling results in extremely low lock ranges for each oscillator, so any process variations in integrated implementations can result in some of the oscillators remaining unlocked due to significant frequency mismatch. We propose two new architectures for a phased-array receiver, which rely on electronically applying the injection signal to each oscillator. This increases the lock range of the ILO and consequently, reduces the effect of process variations between ILOs. The two proposed architectures are illustrated in Fig. 29.4.1, (i) fully-flexible and (ii) meander-line.

The steady-state frequency of an injection-locked oscillator (ILO) is the same as the injection frequency, f_inj, if f_inj is within the lock range of the oscillator (f_L). The steady-state phase difference (φ_ss) between the oscillator output and the injection-signal is given by

\[ \phi_{ss} = \sin \left( \frac{f_{inj} - f_{osc}}{f_L/2} \right) \]

where f_inj is the natural frequency 1/(2πLQ) of the oscillator [5]. The phase difference generated can be varied by controlling f_inj of each individual oscillator. In the fully-flexible architecture, the four ILOs are independently programmable to generate any phase pattern. Nominally, injection locking only generates phases between -90° and 90°. However, an additional 180° phase shift can be attained by flipping the differential terminals, thereby allowing any phase angle between -180° and 180°. The fully-flexible architecture, therefore, allows for arbitrary radiation pattern generation. On the other hand, the meander-line architecture is based on the theory of cascade ILOs. In a cascade of ILOs, each with an equal f_inj, every oscillator output is phase-shifted by φ_inj with respect to the preceding oscillator output. Hence, the output phases are in arithmetic progression, making the architecture an ideal candidate for traditional beam-steering applications. Both of these architectures require good matching between ILOs. They take advantage of the excellent matching and reproducibility of modern day CMOS technology. The prototype chip design has the ability to switch between the two proposed architectures.

Previous implementations of LO phase-shifting architectures in CMOS have applied quadrature VCOs along with variable-gain amplifiers to generate different phases [1,3,6]. Running multiple VGAs at such high frequencies consumes a lot of power. ILOs, on the other hand, inherently amplify the injection signal using regeneration, replacing the mixer buffer, further reducing power consumption. The schematic of the proposed ILO and succeeding CML buffer is shown in Fig. 29.4.2. Signal is injected directly to the negative-gm LC oscillator in the form of current through a gm cell. The incoming injection signal can be switched between the externally-applied signal (fully-flexible architecture) and the previous ILO output signal in the cascade (meander-line architecture). Each oscillator has a continuous tuning range between 1.9 and 2.8GHz with the help of a switched capacitor array and a varactor. The measured lock range and the excellent matching between channels in the digital frequency-tuning characteristics are depicted in Fig. 29.4.3. The maximum frequency difference between any two oscillators in only 20MHz (less than 1% mismatch). With minimal calibration via varactor tuning, the slight mismatch in the oscillator frequencies can be eliminated.

The RF input to each of the receiver channels is downconverted to IF and phase shifted (introduced by the ILO signal) at the output of the mixer. The mixer is a double-balanced modified Gilbert cell with gm boosting for the RF signal (Fig. 29.4.2). The measured gain of the mixer is 11.5dB. The RF input of each mixer is matched to 50Ω using a unity-gain common-gate buffer. The input matching characteristics (S11) for the four channels are shown in Fig. 29.4.4. Subsequently, the IF signals from the four channels are combined in the summer circuit (Fig. 29.4.2).

Of the four RF receiver channels designed, one of the channels showed less than the required individual gain and was not included in our results. Investigation of this issue revealed that this gain reduction can be attributed to the mixer and summer connection for channel 4. The other three channels showed individual gains which were within ±1dB of each other. The maximum total measured gain of the three-channel receiver is 20dB. The SNR improvement due to the three channel phased array architecture is measured to be 9dB. To measure the array radiation pattern, the effect of a receiver-antenna-array feed network was mimicked using RF phase shifters and a 1:4 power divider. Figure 29.4.5 illustrates the measured and theoretical two-channel and three-channel radiation patterns for both architectures. The best-case signal suppression in the null direction is greater than 25dB, whereas the worst-case suppression is about 17/8. The antenna spacing for all these cases is assumed to be half the wavelength corresponding to the RF frequency. Figure 29.4.6 summarizes the measurement results from the chip and Fig. 29.4.7 shows the die micrograph.

References:
Figure 29.4.1: Two architectures for phased-array receivers based on injection locking of oscillators (shaded areas have been implemented on-chip).

Figure 29.4.2: Block diagram and circuit schematics of each RF channel.

Figure 29.4.3: Matching between ILOs: digital frequency tuning of the four oscillators and lock ranges of the four oscillators for different injection powers.

Figure 29.4.4: Input power match of the four RF ports.

Figure 29.4.5: Radiation patterns for fully-flexible and meander-line architectures for different beam directions.

Figure 29.4.6: Summary of measured performance.

Please click on paper title to view Visual Supplement.
Figure 29.4.7: Die micrograph of the fabricated chip in 0.13µm CMOS technology.