A 5GS/s 12.2pJ/conv. Analog Charge-Domain FFT for a Software Defined Radio Receiver Front-End in 65nm CMOS

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Abstract—This work describes the design of CRAFT (Charge Re-use Analog Fourier Transform): an RF front-end channelizer for software defined radios (SDR) based on a 16 point analog-domain FFT. The design relies on charge re-use to achieve 47dB average SNDR on a 5GS/s I/Q input, and consumes only 12.2pJ/conv. Due to its wide-band and low power channelization capabilities, it is expected to reduce the sample rate and dynamic range requirements for wide-band digitization in SDRs.

Index Terms—cognitive radio, CR, FFT, filter, SDR, software defined radio, switched capacitor

I. INTRODUCTION

Conventional software defined radios (SDR) strive to digitize the RF signal and perform spectrum sensing in the digital domain. However, for wideband inputs, this translates to infeasible ADC specifications [1].

A number of techniques including time-interleaving [2] and N-path filter-banks [3], [4] have been proposed to tackle the wideband channelization problem. However, while time-interleaving the ADCs reduces their speed, the input dynamic range (exponentially related to ADC power) remains large. Filter-banks reduce both the speed and dynamic range (by removing out-of-band signals) of ADCs. However, these are based on PLLs, mixers and low-pass filters, and can be considerably power hungry. Additionally, signal reconstruction from the digitized filter-bank outputs is challenging.

In this paper, we propose to use the DFT as a functionally equivalent linear phase N-path filter (see Fig. 1) to perform channelization [5]. This scheme reduces both the speed and dynamic range of the ADCs, and, by virtue of being minimal phase, allows for simple reconstruction in the digital domain. A few current-domain analog DFT filters have been designed recently [6], [7]. However, these designs are speed-limited, and consume significant power (Table I) minimizing the overall gains. In this work, we perform a charge-domain DFT to practically eliminate the power overhead, making a DFT-based wideband digitizing front-end feasible.

This work describes the design of such a DFT filter, CRAFT (Charge Re-use Analog Fourier Transform), based on passive switched capacitors. It performs an analog-domain 16 point DFT running at a 5GS/s input rate and uses only 12.2pJ per conversion. As shown in Fig. 2, an architecture with a CRAFT RF front-end reduces the speed of each ADC by N, at a negligible power overhead. The ADC dynamic range is also reduced due to the removal of out-of-band signals per ADC. The impact of the CRAFT front-end on the ADC power is shown in Fig. 3. The expected total ADC requirements is plotted amongst measured ADC implementations [8]. As seen, the CRAFT front-end brings the required ADC specifications from being infeasible (top right corner) toward being achievable (bottom left half). By solving the broad-band digitizing problem, CRAFT is expected to enable the realization of wide-band SDRs in the future.

II. CRAFT DESIGN CONCEPT

CRAFT operations are based on charge re-use. Once sampled, the charge on a capacitor is shared and re-shared with other charge samples such that the resulting mathematical manipulation is an in-place DFT. By basing the design only on toggling switches (transistor gates), low power and high speeds are enabled. Additionally, the power scales with frequency, supply, and technology in a digital-like fashion.

The in-place CRAFT computations are destructive; therefore, multiple copies of each data value are required for multiple operations. Since a radix-2 FFT algorithm performs the DFT with minimum number of operations per operand per stage (less copies required), it is selected for CRAFT.
The FFT is computed as follows: The input signal is sampled onto capacitors. Since each input is operated on twice in an FFT butterfly, and twice for complex operations, 4 copies of each sample are required. Also, considering I, Q (= 2) and differential (= 2) inputs, the 16 point FFT requires 16 x 2 (complex math) x 2 (butterfly branches) x 2 (I, Q) x 2 (differential) = 256 sampling capacitors.

Only two types of operations are required for an FFT: addition and sub-unity coefficient multiplication. The different charge-based operations performed are shown in Fig. 4. The charges from two capacitors are shared to perform addition. Subsequent sub-unity coefficient multiplication is performed by stealing charge away from the shared output using a suitably-sized capacitor ($C_s$). These techniques are extended to perform complex multiplication, as shown in Fig. 4. An example butterfly operation using multiple complex multiplications is also shown. These butterfly blocks are then used to construct the 16 point CRAFT shown in Fig. 5.

### III. CRAFT IMPLEMENTATION

The CRAFT engine is implemented as shown in Fig. 6. The figure closely emulates the layout implementation. A layout screenshot of the core is shown on the right.

a) Sampler: As shown in Fig. 6, each input sample is stored using a set of 16 capacitors (4 copies of differential, complex inputs). For a 16 point FFT, 16 such sets (total of 256 capacitors) are used. The 256 sampling switches are designed to run at 5GS/s with a single-ended input swing of $\pm 300mV$ ($V_{pp, dif} = 1.2V$) and a 60dB SFDR in simulation. The sampling capacitors are sized at 200fF each such that the per-bin output referred $kT/C$ noise contribution by the CRAFT engine due to the sampling and processing operations is 65dB below the output full-scale signal.

As shown in Fig. 6, 16 buses, each 16 wide, are connected to the sampling capacitors, and run through the CRAFT core. These wires are always connected to the sampling capacitors; consequently, their parasitic capacitance forms a part of the sampling and needs to be accurately matched. Additionally, since the operations are performed in-place, the outputs appear on the sampling capacitors at the end of the processing phase.

b) CRAFT core: The CRAFT core performs the FFT operation in $4 (= log_2(16))$ stages as represented in Fig. 5. As described in Fig. 4, each butterfly is implemented using switches and scaling capacitors that perform a set of share and multiply operations on the input samples. The switches and wires are sized to provide $7\tau$ settling at 5GS/s.

The 4 stages of CRAFT operation are shown in Fig. 6. In stage 1, the neighboring buses share their charge. In the second stage, share and scalar multiply operations are performed. Multiplication by $(\frac{\sqrt{2}}{2} + j\frac{\sqrt{2}}{2})$ is performed in a single step (unlike as shown in Fig. 4) by exploiting $m = m_c$. This increases settling time, and minimizes attenuation. In the third stage, share and multiply operations based on the butterfly operation in Fig. 4 are performed. Again, prior knowledge of the coefficients is utilized to minimize attenuation. The fourth stage performs a share operation. Using the improvised share and multiply techniques, only 5 clock phases are used for FFT computation. Moreover, the total attenuation is limited to 0.38 (12X superior to an unmodified implementation).

Note that the Fig. 6 FFT implementation imitates the signal flow shown in the last row of Fig. 4; as a result, after each operation, half the wires return to their bus while the rest continue on the other bus. To equalize the wiring parasitics, switches are placed midway between two operand buses. Two example wires, one always returning to its bus, while the other always shifting on to the other operand bus, are highlighted in the layout screenshot in Fig. 6. As seen, the two wire lengths (and their parasitics) are nominally matched.

c) Output latch: On the far end of the core, the wires connect through switches to 32 ($16 \times 2$ for real and imaginary) OTA based analog latches that save the outputs prior to being read out (Fig. 6). To match the CRAFT performance, a two-stage, folded-cascode, differential OTA with 70dB gain and 1GHz UGB is designed.
d) State machines: As shown in Fig. 7, the sampling, core, and testing interface require multiple clocks to be generated. The design uses an input clock to generate internal signals. State machine 1 (SM1) is externally triggered and generates 16 sampling clock phases. It then generates the processing clocks that operate the core switches. Another state machine (SM2) uses handshaking with SM1 and with an external FPGA (NI-7811R) to determine if the outputs and the FPGA are ready and subsequently generates the analog latch clocks. The latched outputs are observed sequentially using an FPGA controlled output MUX.

As expected, the design relies heavily on digital circuits. Also the design’s regularity and complexity make it comparable to digital designs. However, the CRAFT engine is an analog circuit, and remains vulnerable to circuit non-idealities including noise, matching, and non-linearity. Consequently, accurate modeling of non-idealities is critical. Moreover, switched capacitor circuit noise, charge-injection, and charge-accumulation are not well-modeled in circuit simulators. For this design, CRAFT-specific models of non-idealities were developed. A priori knowledge of operations was exploited to devise novel circuit techniques such as correlated noise reduction, and differential settling error cancellation. Performance was optimized using system simulations enabling the high dynamic range, even at 5GS/s.

IV. MEASUREMENT RESULTS

The design has been implemented in the IBM 65nm CMOS process. Measurement results are shown in Fig. 8–11. Fig. 8 shows the CRAFT outputs with a 312.5MHz (= \( \frac{3GHz}{16} \)) single-tone input at 5GS/s. Curve I shows the measured output magnitude across 16 bins. Ideally, all bins except bin 1 should be at the noise floor, but due to systematic inaccuracies in parasitic extraction, uncompensated interconnect capacitances on the stealing capacitors of this CRAFT version resulted in FFT twiddle factor errors. This causes a systematic input-independent computation error. This inaccuracy is estimated in measurement using a training sample, and used for offline digital correction. Subsequent plots in this paper use the corrected values. Curve II in Fig. 8 shows the corrected plot depicting the circuit noise floor at -46dB. The test setup noise floor is at -48dB as shown. To explore the non-linearity floor, a synchronous average over 500 measurements was used. The resultant Curve III shows the non-linearity floor with 48dB SNDR per bin and 43dB SFDR. The non-linearity predicted by our system level simulations is shown in Curve IV. The discrepancy with Curve III is attributed to non-idealities in the AWG generated inputs (8 bit resolution).

The SNDR at 1, 3, and 5 GS/s for a single-tone input frequency placed at different bins is shown in Fig. 9(a). The average SNDR across these input frequencies is \( \approx 50dB \) at 1 and 3 GHz and degrades to 47dB at 5GHz; SNDR better than 45dB is maintained across all frequencies. This provides 7-8 bits of spectrum sensing resolution over a 5GHz (2.5GHz×2 due to I, Q) frequency range in the digital back-end.

Output SNDR with varying input amplitudes at 5GS/s are shown in Fig. 9(b). A fourth-order fit shows a linear SNDR improvement with increasing amplitude before being limited by circuit non-linearities. Results from a two-tone test with tones on adjacent bins are shown in Fig. 10. Two single-tone measurements and their superposition (adjusted to the sampler input full-scale) are also shown. The difference between the superposition and the measured two-tone output is indicative of the additional non-linearity introduced. The relative increase in bins 13 and 14 is likely due to uncorrected twiddle factor errors in stage 2 of the CRAFT engine.

As depicted in Fig. 11, measurements clearly show the expected digital-like relationship of the CRAFT energy with frequency and supply voltage. As a result, CRAFT is expected to respond favorably to technology scaling.
V. Conclusion

This work describes a wideband ultra-low power RF front-end channelizer incorporating a 16 point FFT. The design is based on charge re-use enabling it to run at speeds of 5GS/s with a 47dB SNDR, while consuming only 12.2pJ/conv.

Table I compares the CRAFT performance with one digital and two analog-domain FFT implementations. As shown, for comparable SNDR values, CRAFT operates at speeds 5X faster than previous state-of-the-art designs. Additionally, it consumes better than 28X lower energy. As an RF channelizer, it is expected to reduce digitization requirements enabling wide-band digital spectrum sensing. As a result, it helps advance the state-of-the-art for wide-band SDR architectures.

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REFERENCES