Dual Channel Injection-Locked Quadrature LO Generation for a 4GHz Instantaneous Bandwidth Receiver at 21GHz Center Frequency

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Abstract—This paper presents an LO generation scheme for a 21GHz center-frequency, 4GHz instantaneous bandwidth channelized receiver. A single 1.33GHz reference source is used to simultaneously generate 20GHz and 22GHz LOs with quadrature outputs. Injection locking is used instead of conventional PLL techniques allowing low-power quadrature generation. A harmonic-rich signal, containing both even and odd harmonics of the input reference signal, is generated using a digital pulse slimmer. Two ILO chains are used to lock on to the 10th and 11th harmonics of the reference signal generating the 20GHz and the 22GHz quadrature LOs respectively. The prototype design is implemented in IBM’s 130nm CMOS process, draws 125mA from a 1.2V supply and occupies an active area of 1.8mm².

I. INTRODUCTION

With the advent of wireless technology the demand for higher data rates has continued unabated. According to Shannon’s capacity theorem [1], the channel capacity increases linearly with bandwidth, and only logarithmically with SNR. Therefore, increasing the bandwidth is the most effective way to achieve higher data rates. This poses several challenges to the RF receiver, the most prominent of which is the ADC design. Higher bandwidths imply a high ADC clocking speed as well as a high dynamic range making the ADC power-hungry and difficult to design, if at all feasible. An effective way to overcome this problem is to use frequency sub-channelization, whereby the wide bandwidth is divided into smaller sub-bands. Besides reducing the clocking speed of the ADC, sub-channelization also increases the immunity to narrow-band interferers reducing the ADC dynamic range requirements [2]. The number of ADCs increases but their individual sample rates decrease. Although the reduced sample rate simplifies the ADC design, the increased number of ADCs would result in the same total power consumption [3]. Fortunately, channelization also reduces the number of independent in-band signals hence reducing the peak to average power ratio (PAPR) [4], further reducing the ADCs dynamic range requirements. Consequently, the overall power consumption goes down.

A channelized receiver, capable of achieving 4GHz of instantaneous bandwidth, around a 21GHz center frequency, is shown in Fig. 1. An external wideband LNA amplifies the entire band. The wideband signal is then down-converted in the frequency domain into two 2GHz channels using two sets of quadrature mixers, operating at 20GHz and 22GHz. Two sets of lowpass filters complete the channelization for this dual direct conversion receiver. Digitization can be performed by using a high-speed ADC in each I/Q channel [5], or by further channelization in the baseband using an analog FFT [6]. The desired wideband signal can then be reconstructed digitally by upsampling each digitized stream by two and the use of digital reconstruction filters to account for filter phase and amplitude effects [2].

A major challenge for the receiver in Fig. 1 is the generation of two phase synchronous quadrature LOs at 20GHz and 22GHz. In [7], the quadrature 4GHz output of a PLL is mixed with the 0.5GHz quadrature output (obtained by dividing the PLL output) using single-sideband (SSB) mixers to generate 3.5GHz, and 4.5GHz quadrature LOs. At mm-wave frequencies, this approach is inefficient; high frequency dividers and SSB mixers are power hungry. Moreover, mixer linearity is limited at mm-wave frequencies resulting in a large number of spurious components.

Injection locking is an alternative approach for LO generation in mm-wave designs [8]–[11]. Most designs, however, are aimed at a single LO. The design in [8] implements simultaneous LOs but it has two drawbacks: it is not capable of quadrature signal generation and it can only generate integer multiples of the reference signal. Hence, a different approach needs to be used for a more generalized solution.

This paper addresses the use of injection locking to simultaneously generate 20GHz and 22GHz phase synchronous quadrature LOs using a single 1.33GHz reference. Section II provides system overview and circuit implementation details. Section III presents measurement results and discussion. Finally, section IV outlines overall conclusions.

II. SYSTEM AND CIRCUIT OVERVIEW

Two ILO chains are used to generate 20GHz and 22GHz quadrature LOs as shown in Fig. 1. The 10th and (n + 1)th harmonics of the reference are bandpass filtered then divided by two to generate quadrature outputs. This results in high quality quadrature generation with reduced power consumption: the dividers operate at a frequency lower than the final LO frequency. Note that the same technique for quadrature generation
in a PLL requires the dividers to operate at double the target LO frequency. The quadrature outputs are further multiplied using quadrature frequency triplers, generating $\frac{3}{n} f_{ref}$ and $\frac{3}{n}(n+1) f_{ref}$ LOs. To generate 20GHz and 22GHz, $n = 10$ and $f_{ref} = 1.33GHz$ are chosen.

Each ILO chain consists of a pulse-slimmer, a bandpass filter (BPF), an injection locked frequency divider (ILFD) and an injection locked frequency multiplier (ILFM). The pulse slimmer generates a harmonic-rich signal that is digitally shaped to emphasize the $10^{th}$ and $11^{th}$ harmonics. In the 20GHz path, a BPF tuned to the $10^{th}$ harmonic (i.e. 13.33GHz) suppresses the other undesired components. An ILFD follows the BPF, dividing its output by two to generate quadrature outputs at 6.66GHz. The quadrature outputs are fed to an ILFM which triples the 6.66GHz quadrature input, generating 20GHz quadrature outputs. The outputs are fed to downconversion mixers for testing purposes. Similarly, the 22GHz chain begins with a 14.66GHz BPF ($11^{th}$ harmonic), followed by a 7.33GHz ILFD, then a 22GHz ILFM.

The digital pulse slimmer (PSLIM) is shown in Fig. 2. The section preceding the NAND gate generates a square-wave with a 1/8 duty cycle which is optimal for enhancing the desired $10^{th}$ and $11^{th}$ harmonics. Fine delay for this purpose is added by means of a MOS resistor in the signal path. A semi-digital differentiator, consisting of two chains with different delays, follows the NAND gate to further enhance the desired harmonics. The differential output of the differentiator takes the form $(1 - z^{-1}) s(t)$, which is a differentiated version of the input signal $s(t)$. The inherent low-pass nature of the digital chain results in an overall bandpass response.

The bandpass filter (BPF) shown in Fig. 3 has to achieve two basic functions. First, it has to amplify the desired harmonic to a level that allows the following stage to injection lock with a reasonable lock range. And second, it has to provide sufficient suppression of the close-in undesired harmonics. Both functions are efficiently achieved using an ILO. Under free-running conditions, the ILO acts as an oscillator whose amplitude ($V_{osc}$) has a finite value. Once locked, the output amplitude remains the same creating an effective gain of $V_{osc}/V_{inj}$, $V_{inj}$ being the injected signal’s amplitude. Moreover, a spur at an offset $f_{inj}$ from the injection signal would be suppressed by $f_{inj}/f_{lo}$ [12], where $f_{lo}$ is the single-sided lock range. This suppression is higher than that obtained using a passive LC tank of the same Q. In fact, SpectreRF® simulations show that the effective Q of the ILO-based BPF is almost twice that of the passive LC tank, when both are fed with the pulse-slimmed signal. Two ILO-based BPFs are designed for the 20GHz and 22GHz chains, with center frequencies of 13.33GHz and 14.66GHz respectively. Each ILO draws 4mA from a 1.2V supply.

The injection-locked frequency divider (ILFD) is shown in Fig. 4 and is based on the design in [13]. Unlike [13], however, injection is not performed at the tail current source. Since no buffer is used between the BPF and the ILFD, injection at the tail source presents a large load capacitance to the BPF increasing its power consumption considerably. To avoid this, direct injection is used as suggested in [14]. An NMOS switch is added in parallel to the oscillator’s LC tank. For our design, the switch is biased such that it switches on only once during a whole cycle of the injection signal. The switch’s input capacitance is roughly 25 times smaller than the tail current transistor, simplifying the design of the preceding BPF. Two ILFDs are designed, a 6.66GHz ILFD for the 20GHz chain and a 7.33GHz ILFD for the 22GHz chain; each consumes 27mA from a 1.2V supply (buffers included).

The injection locked frequency multiplier (ILFM), acting as a tripler, is shown in Fig. 5 [15]. The injection differential pair is biased in subthreshold, and is operated in class-B mode resulting in a strong third harmonic current component that is comparable to the fundamental. An added advantage of subthreshold operation is the reduced power consumption in the injection pair. Two ILFMs are designed, with 20GHz and 22GHz center frequencies. Each consumes 29mA from a 1.2V supply.

In each ILO along the chain, two bits are used for coarse switched-capacitor frequency tuning using binary-weighted MIM caps. Hyperabrupt PN junction diodes are used for fine frequency tuning. To ensure operation in the desired frequency band and proper startup, the parasitic inductance and
AC resistance of the interconnects in all the oscillators were extracted using Integrand’s EMX® EM-simulation tool [16].

III. MEASUREMENTS AND DISCUSSION

The chip was fabricated in IBM’s 130nm CMOS technology. The chip micrograph is shown in Fig. 6. The active area is 1.8mm². A reference 1.33GHz signal is supplied using an HP E4436B signal generator. An on-chip 50Ω resistor provides termination for the generator. The quadrature oscillator outputs are measured using GSSG probes and the output is displayed on an HP E4407B spectrum analyzer where the spur levels and phase noise are measured. The GSSG probes are driven by on-chip 50Ω buffers. Each chain consumes around 63mA from a 1.2V supply, for a total current consumption of 125mA. The current consumed by each block is detailed in Table I.

The measured phase noise of the 20GHz and 22GHz LOs is shown in Fig. 7 and Fig. 8 respectively. The out-of-band spurs are at 1.33GHz offset and the in-band spurs are at 666MHz (1.33GHz/2) offset. In the 22GHz chain the pulse slimmer’s spurs are highly attenuated at the BPF’s output except for the 10th, 11th and 12th harmonics. In the following ILFD, the 11th harmonic causes locking generating the 7.33GHz output. The 10th and 12th harmonics undergo two operations: they are divided by two, with a highly attenuated output, generating the 666MHz-offset spurs and they are mixed with the ILFD’s output generating the 1.33GHz-offset spurs. The ILFD’s output is then mixed up to 22GHz through the ILFM. In the 20GHz chain, the significant harmonics at the BPF’s output are the 9th, 10th and 11th harmonics. The final 20GHz output is generated by locking to the 10th harmonic, whereas the spurs are generated by the 9th and 11th harmonics in a way similar to that of the 22GHz chain.

As shown in Fig. 10, the 22GHz chain achieves an in-band spur suppression better than 46dBc and an out-of-band suppression better than 37dBc. In the 20GHz chain, on the other hand, the in-band spurs are suppressed to a level lower than the measurable noise-floor (around -55dBc) whereas the out-of-band spurs are suppressed by more than 37dBc.

IV. CONCLUSIONS

In this work an LO scheme for generating simultaneous phase synchronous quadrature LOs was presented for a
Channelized receiver. The developed architecture can be easily extended to more than two channels, and can be implemented at different frequencies. This provides a viable mechanism to realize mm-wave sub-channelized receivers. To the best of our knowledge, this is the first paper to present simultaneous mm-wave LOs with quadrature outputs and small frequency separation. This is evident from the comparison in Table III. Reference [8] provides simultaneous LOs but no quadrature capability. Moreover, it needs a high frequency reference source and only generates integer multiples of that source. Reference [11], on the other hand, provides quadrature outputs tunable from 5–32 GHz but not simultaneous LOs. Finally, reference [7] provides simultaneous quadrature LOs but at lower GHz range. The prototype occupies 1.8mm² in 130nm process, drawing 125mA from a 1.2V supply. Phase noise matches the upconverted reference’s noise up to 1MHz offset. In-band spurs are suppressed by more than 46dBc and out-of-band spurs by more than 37dBc. The presented design is flexible and can be optimized for lower power, better phase-noise or higher frequency depending on the application needs.

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References