A 52% Tuning Range QVCO With a Reduced Noise Coupling Scheme and a Minimum FOM$_T$ of 196dBc/Hz

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Abstract—A wide-tuning range QVCO with a novel complimentary-coupling scheme is presented. Two NMOS-only VCOs are coupled via complimentary PMOS injection transistors. This shifts the injection current away from the zero-crossings of the output voltage, thereby reducing the sensitivity of the VCO to injection noise, which results in significant phase-noise improvement. Phase-shift is achieved without frequency-dependent phase-shifting networks, allowing robust coupling over a wide tuning range. As a proof-of-concept, a prototype is designed in TSMC 65nm process with 4-bits of discrete tuning spanning the frequency range 4.6-7.8 GHz (52% tuning range). The prototype operates from 0.5V supply, with a power consumption ranging from 7.4mW–11mW, while achieving a minimum figure-of-merit (FOM) of 181.6dBc/Hz, and a minimum FOM of 196dBc/Hz.

I. INTRODUCTION

Quadrature LO generation is crucial to the operation of direct-conversion transceivers. Conventionally, quadrature generation utilizes either divide-by-two frequency dividers, or polyphase filters [1]. In particular, divide-by-two dividers require the system’s oscillator to work at double the desired frequency, resulting in an overall increase in power consumption. Polyphase filters, on the other hand, are lossy requiring more power consumption for buffering and amplification. Moreover, multistage polyphase filters are often employed to combat process variations, causing additional losses.

The basic structure of the LC-based QVCO is shown in Fig. 1. Two LC VCOs are coupled via complimentary PMOS injection transistors [3]. This shifts the injection current away from the zero-crossings of the output voltage, thereby reducing the sensitivity of the VCO to injection noise, which results in significant phase-noise improvement. Phase-shift is achieved without frequency-dependent phase-shifting networks, allowing robust coupling over a wide tuning range. As a proof-of-concept, a prototype is designed in TSMC 65nm process with 4-bits of discrete tuning spanning the frequency range 4.6-7.8 GHz (52% tuning range). The prototype operates from 0.5V supply, with a power consumption ranging from 7.4mW–11mW, while achieving a minimum FOM of 181.6dBc/Hz, and a minimum FOM of 196dBc/Hz.

This “varactor-like” effect leads to flicker-noise upconversion, adding $1/f^3$ phase-noise [6]. Several techniques have been proposed in literature to alleviate these drawbacks. In [7], anti-phase coupling of the common-source nodes of the two VCOs is done via an inverting transformer. Since the common-sources oscillate at twice the fundamental frequency, this makes the two VCO outputs in quadrature. This eliminates the coupling transistors altogether, improving phase-noise. For proper coupling, however, large swings are needed at the common-source node, limiting the tuning range. In [1], the coupling transistor is inserted in series with the negative-$g_{m4}$ transistor. This limits the headroom, and requires a large coupling transistor that loads the oscillator, limiting the tuning range. In [8], coupling is done through the bulk terminal of the $g_{m4}$ transistor, with the drawback of a reduced Q due to occasional forward-biasing of the bulk-source and bulk-drain junctions. In [9], coupling is performed by transformers, eliminating the coupling transistors. This comes with the drawback of larger transformer area, as well as increased design complexity.

LC QVCO performance can also be improved through the use of a phase-shift ($\Delta \varphi$) in the injection path [6], [10]. Ideally, a $\Delta \varphi$ of 90° would make the injection current coincide with the peak of the output voltage, resulting in a minimal phase-noise penalty [4]. It would also cause the QVCO frequency to coincide with the tank frequency, maximizing the Q-factor and eliminating the “varactor-like” effect and its consequent $1/f^3$ phase-noise. In practice, however, a 90° phase-shift is hard to achieve. Nevertheless, a reasonable phase shift (in the order of 40°–50°) helps decrease the phase noise [6]. Previous phase-shift implementations either depend on frequency sensitive passive phase-shifting networks [6], [10], or employ frequency-insensitive shifting that loads the tank [11].

In this paper, a simple and robust method of implementing the coupling phase-shift is presented. Unlike the previously reported implementations, the proposed technique is frequency-insensitive allowing quadrature operation over a wide tuning range, without loading the tank. Section II provides an overview of the proposed technique. Section III presents measurement results. Section IV provides conclusions.
II. CIRCUIT OVERVIEW

The core of the proposed QVCO is a simple cross-coupled LC VCO, with the tail source removed to reduce the $1/f^3$ noise [4], [12]. An inductor is placed at the common-source to resonate with the total parasitic capacitance at that node, at twice the oscillation frequency $2f_0$. This helps avoid Q factor degradation at high swing hence improving the overall phase-noise performance [12].

The full schematic of the proposed QVCO is shown in Fig. 2. The QVCO is formed by coupling two of the core VCOs. It resembles the direct-coupled QVCO of Fig. 1 with one difference; the coupling transistors are PMOS instead of NMOS transistors. While this might seem to shift the injection current by $180^\circ$ making the proposed QVCO very similar to the basic QVCO, the simple intuition is flawed.

This can be explained with the help of Fig. 3 which shows the large-signal time-domain waveforms of the coupling transistors over one oscillation cycle. Both $V_g$ and $V_d$ of coupling transistors sit at $V_{dd}$ in absence of oscillations. In the oscillation mode, the $V_g$ and $V_d$ voltages are in quadrature as they represent the single-ended quadrature outputs of the oscillator. Injection only happens when $V_{sg}$ is greater than the threshold voltage. However, at the peak $V_{sg}$ voltage (where transistors should be the most conductive), the $V_{sd}$ voltage is zero, thus forcing the $I_{sd}$ current to zero. Hence, injection current is forced to be zero at the zero-crossings of the oscillator. Current is injected when $V_{sg} > |V_{th}|$ and $V_{sd}$ is non-zero as shown in Fig. 3, resulting in current pulses far from the zero-crossing point.

As an added advantage, PMOS devices have inherently lower flicker noise than their NMOS counterparts due to the buried nature of the channel. The drawback is that PMOS devices need to be larger than NMOS devices for equal injection strengths. This becomes a problem only when the active devices constitute a large percentage of the total tank capacitance.

To verify the phase-shifting effect, simulations are made to compare the proposed QVCO (of Fig. 2), with a similar QVCO that has the PMOS coupling transistors (green transistors in Fig. 2) replaced with NMOS transistors. Since NMOS transistors have higher mobility than PMOS transistors, and to ensure a fair comparison, the NMOS transistors are sized such that their total injected charge (integration of the injected current over time) is equal to their PMOS counterparts. Both oscillators are tuned to operate at the same frequency of 8GHz.

Fig. 4 shows the injection current waveform overlapped with the output voltage waveform for PMOS coupling. It can be clearly observed that the injection current is very small at the voltage zero-crossings, and goes to a maximum away from the crossing. In fact, the peak current is shifted from the voltage zero-crossing by around $55^\circ$, with no explicit phase-shifting.
network employed. The same waveforms for the NMOS case are shown in Fig. 5, showing that the injection current peak almost coincides with the output voltage zero-crossing. The peaks are not perfectly aligned; there is a finite phase-shift of around 10°.

Phase-noise simulation is done for both PMOS coupling and NMOS coupling using SpectreRF® at the same frequency of 8GHz. As evident from Fig. 6, the PMOS coupled QVCO has a significantly better phase noise performance than its NMOS counterpart over three decades of frequency offset. The PMOS coupled version is better by 6dB in the $1/f^3$ region, and better by up to 8dB in the $1/f^2$ region.

III. MEASUREMENTS AND DISCUSSION

A prototype was fabricated in TSMC’s 65nm CMOS process. Discrete tuning of the frequency is employed, using 4-bit binary-weighted switched MIM capacitors. The design occupies an active area of 0.67mm$^2$. The buffered QVCO outputs are connected to GSSG pads for on-chip probing, using 50Ω buffers. The chip micrograph is shown in Fig. 7.

The QVCO was tested at three supply voltages: 0.42V, 0.5V and 0.6V. Due to the absence of the tail source, power consumption scales with the supply. It was observed that increasing the supply voltage above 0.5V increases power consumption with little phase-noise improvement. Hence, a 0.5V supply is provided to the oscillator through an off-chip regulator, and is used throughout the measurement. The 0.5V supply is used for the oscillator core, while the switches of the capacitor array use a 1V supply for lower series resistance, and effectively a higher capacitor Q.

The oscillator’s output is measured through a GSSG probe. The differential probe output is connected to an off-chip balun for differential to single-ended conversion and the single-ended output is fed to a R&S FSW43 spectrum analyzer for frequency and phase-noise measurement. Outputs are also downconverted and fed to an Agilent 81204B oscilloscope.

The output frequency versus tuning word for the QVCO is shown in Fig. 8. The QVCO can be tuned from 4.59GHz to 7.82GHz achieving a frequency-tuning range (FTR) of 52%. Fig. 8 also shows the measured power consumption of the QVCO versus the tuning word. Power consumption decreases for higher output frequencies (lower tank capacitance), and vice versa. The power consumption ranges from 7.36mW at the highest frequency, to 10.98mW at the lowest.

The measured phase-noise of the QVCO at the center frequency of 6.24GHz, is shown in Fig. 9.

The measured phase-noise for 1MHz and 3MHz offsets, across the tuning range, is shown in Fig. 10. At 3MHz offset, phase-noise ranges from -123.5dBc/Hz to -128.5dBc/Hz across the tuning-range, while the phase-noise at 1MHz offset ranges from -111.5dBc/Hz to -117.8dBc/Hz across the tuning-range.

The FOM (for 3MHz offset) is shown in Fig. 11. The FOM touches 185.4dBc/Hz at its peak, and goes down to
The large tuning range in [14] is achieved through the use of transformers; the tuning range in this work is achieved using conventional tanks with no transformers. Moreover, the FOM, as well as FOM$_T$, of this design is higher than that in [14]. Designs in [7], [10], [13] achieve higher FOM, but also use higher supplies. The design in [9] achieves a higher FOM with a 1V supply but, with the added design complexity and area of using coupling transformers.

This work shows that by replacing NMOS coupling transistors (in an NMOS-only QVCO) with PMOS transistors, state-of-the-art FOM performance can be achieved with a simple, robust design that uses conventional tank-circuits. Moreover, state-of-the-art tuning-range is achieved, with best-in-class FOM$_T$ performance.

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