High Linearity PVT Tolerant 100MS/s Rail-to-Rail ADC Driver With Built-in Sampler in 65nm CMOS

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Abstract—A novel completely inverter-based ADC driver is proposed that relaxes the gain and unity gain bandwidth requirements of the negative feedback loop by making it not see the closed loop gain. This ADC driver has a built-in first order anti alias filter and uses a passive amplifier to provide a rail-to-rail sampled output signal. This design exploits the linearity of current mirrors and achieves 65dB of linearity at the Nyquist rate for a rail-to-rail output. A semi-constant current biasing circuit for inverters has been proposed to minimizing PVT variations in lower technologies. As a proof of concept an ADC driver is designed and implemented in TSMC’s 65nm GP CMOS technology. The measured design operates at 100MS/s and has an OIP3 of 40dBm at the Nyquist rate, provides a gain of 8, and samples the signal onto a 1pF output capacitance while drawing 2mA from a 1V supply.

I. INTRODUCTION

Battery-powered applications naturally demand low power. Mobile video and high-definition television applications require high-speed, medium resolution, and low-power design specifications, which are the realm of pipelined and SAR ADCs. The SAR ADC has become increasingly popular as it is based on switching rather than amplifying, contains less hardware than other topologies and it scales well with technology. However, due to its inherent high input capacitance the design of the input driver is becoming more difficult, especially at lower technology nodes [1]. Logic circuits’ static power dissipation limit the scaling of threshold voltages of transistors. The noise requirements of an operational transconductance amplifier (OTA) design becomes increasingly more stringent for lower input voltage swings. Linearity requirements demand high overdrive voltages on the input transistors of the OTA which is limited by the power supply, however, high overdrive voltages results in higher noise for the same current.

Rail-to-rail inputs for an ADC reduce its power consumption while simultaneously increasing the dynamic range. Ring amplifiers [2] are a topology that can give rail-to-rail swing at the cost of increased noise. Passive amplification techniques [1], [3] have demonstrated an ability to amplify signals to rail-to-rail levels at the cost of increased loading on the driver. An ideal ADC driver should be able to amplify the input signals to rail-to-rail voltages and sample the signal onto the input capacitor of the ADC. The requirements on the OTA gain-bandwidth product (GBP) and DC gain keep increasing with increased closed loop gain. Inverter-based designs are becoming the preferred topology at lower technologies nodes due to their higher $g_m/I_D$ efficiency [4].

In this work we present an ADC driver which employs a current-mirror based architecture. Voltage-to-current conversion is done using a passive device and a negative feedback circuit and the current is amplified by a current-mirror [5]. A trans-impedance amplifier (TIA) converts this current back to a voltage with half $V_{DD}$ swing. A passive RC circuit is used as a first-order anti-alias filter (AAF) before sampling is performed. Passive amplification is employed to amplify the signals to rail-to-rail levels [3]. We also show that the gain bandwidth product (GBP) and the DC gain of the negative feedback loop are not affected by the closed-loop gain. Inverters are used as amplifiers in this design and the nmos devices in the inverters are biased at a constant current resulting in low PVT variations.

This paper is organized as follows. Section II presents the ADC driver architecture. This is followed by a discussion on the current-mirror and the trans-impedance amplifier design in Section III. Section IV describes the biasing of the transistors. Finally, measurement results are presented in Section V.

II. ADC DRIVER ARCHITECTURE

The architecture of the proposed ADC driver is shown in Fig. 1. The input voltage is converted to a current using a passive resistor and negative feedback. This current is then fed to the current-mirror where amplification is performed. The amplified current is then converted back to voltage by a trans-impedance amplifier for a half $V_{DD}$ swing. A passive anti-alias filter is used to filter the noise above the 3-dB bandwidth of the TIA after which sampling is performed. The final amplification is done passively for better linearity. For an amplifier with perfect efficiency the power required to charge a capacitor is

$$ P = \frac{1}{2}CV^2f $$

(1)

It can be seen from Eqn. 1 the power required to charge a capacitor ($C$) to a voltage $V$ is the same as charging a capacitor ($4C$) to $V/2$. However, charging the capacitor to $V/2$ swing affords a linearity advantage to the amplifier. This principle is used and then followed by passive amplification to result in a rail-to-rail output swing which is ready for the ADC (or is the SAR ADC capacitor itself).
Fig. 2 shows the detailed circuit diagram for the ADC driver, the V-to-I, the current-mirror, the TIA, the RC AAF, the passive-amplifier and sampler that were shown in Fig. 1.

### III. COMPONENTS OF THE ADC DRIVER

#### A. Current Mirror Design

The input voltage is converted to a current using a passive resistor $R$ and the negative feedback circuit including $OTA_1$, as seen in Fig. 2. $OTA_1$ is designed as a cascade of two biased inverters as shown in Fig. 3. All the inverters used in this design are multiples of the unit bias inverter and therefore track with the PVT variations. Inverters have the advantages of the best $g_{m}/I_D$ efficiency while supporting a high linear operating range for an appreciably large voltage swing. The common mode voltage $V_M$ is the meta stable voltage of the inverters. The signal $V_{CM}$ comes from the biasing circuit as explained in Section IV. The input referred noise of the current mirror is given by

$$\begin{align} 
\gamma v^2_{n,1} &= 4kTR \left( 1 + \frac{g_{m,\text{inv}}R}{1 + \frac{1}{m}} + \frac{\gamma(1 + \eta)}{g_{m,OTA1}R} \right) 
\end{align}$$

As seen in Eqn. 2, the trans-conductance of the inverter ($g_{m,\text{inv}}$) must be small and that of the OTA ($g_{m,OTA1}$) must large for low noise. Hence, the input inverter is designed to have a lower aspect ratio thereby consuming lower current. Since gain is obtained by mirroring this inverter, the overall power is also minimized. The $OTA_1$ is designed for a higher trans-conductance for low noise and high loop gain.

Non-linearity in the current mirror is due to $g_m$ and $g_{ds}$ non-linearity of the transistors. Any $g_m$ nonlinearity in the input inverter is reflected by a change in the output voltage of $OTA_1$. As the output inverter has the scaled size ($m$) of the input inverter, any $g_m$ nonlinearity that is introduced gets canceled. Since both the drains of the input and output inverters are held at the same common mode voltage the differences in their respective $g_{ds}$ non-linearity is greatly reduced. Additionally, differential or pseudo-differential implementations suppress even order harmonics. The effectiveness of this non-linearity cancellation relies on the matching of the transistors. Therefore, these inverters are carefully laid out using common-centroid techniques to reduce any systematic mismatch.

#### B. Trans-impedance Amplifier (TIA) Design

The trans-impedance amplifier is designed using three biased inverters as $OTA_2$ (Fig. 3) with a feedback resistor. The amplified current from the current mirror is converted back to voltage by the feedback resistor ($nR$). Since the current-mirror inverter providing the input is designed for low current (for low noise purposes), it has a higher output impedance than the feedback resistor ($nR$) of the trans-impedance amplifier. The input referred noise of the trans-impedance amplifier is

$$\begin{align} 
v^2_{n,2} &= 4kTR + \frac{v^2_{n,OTA2}}{nR} 
\end{align}$$

where $v_{n,OTA2}$ is the input-referred noise of $OTA_2$. Fig. 4 shows the comparison of a trans-impedance amplifier and an inverting amplifier. The OTA noise ($v^2_{n,OTA}$) sees a gain of $1+n$ in the inverting amplifier and one, 1, in the trans-impedance amplifier due to the high impedance of the current source. Hence, $OTA_2$’s noise is not amplified to the output but the signal gets amplified by the feedback resistor. Since the gain is given as $n$, larger resistors give higher gain as well as increased noise keeping the $OTA_2$’s noise contribution constant.

The first stage in $OTA_2$ is designed with a large overdrive voltage for linearity reasons. In the TIA the OTA gain and bandwidth are not affected by the feedback factor, unlike for an inverting amplifier, which allows a 10dB improvement in GBP and DC gain which yields a 28dB improvement in the IMD for a closed loop gain of $n = 2$.

#### C. Anti-Alias Filter

The gain bandwidth product of the negative feedback loop is much greater than the signal frequency resulting in better linearity suppression up to the band-edge frequency. If this signal is sampled directly at Nyquist all the noise past the Nyquist signal bandwidth aliases into the signal band. In this work, we remedy this using a passive RC circuit to do a first-order anti-alias filter utilizing $R_f$ in Fig. 2 and the sampling capacitors. The 3dB bandwidth of the RC circuit is selected to be two times the signal bandwidth to have minimal residual attenuation at the band edge frequency while filtering an appropriate amount of noise. Since it is a passive circuit, it doesn’t deteriorate the linearity of the circuit. This resistor also
servers as the compensation of the loop as the resistor in series with sampling capacitor creates a left half-plane zero which increases the phase margin of the loop. It also reduces any effects of switching transients from the sampler onto OTA

**D. Sampler**

The input signal to the sampler is half \( V_{dd} (1V_{pp-diff}) \) and is sampled on a 4pF capacitor at 100MS/s to be used for passive amplification at a later stage. Two samplers copies are clocked in a ping-pong fashion to maintain a constant OTA load.

**E. Passive Amplification**

Passive amplification is employed to get a rail-to-rail output [3]. The passive amplifier introduces less noise \((kT/C)\) compared to an active amplifier \((\eta kT/C\), where \(\eta\) is the excess noise factor of the active amplifier\) and is also inherently highly linear. The passive amplifier provides common-mode rejection and sets the output common-mode voltage to the ADC at half \( V_{dd} \). In addition, it achieves an area reduction of the sampling capacitor and requires no reference voltage.

In this design a gain of 8 is distributed among the current mirror, TIA and the passive amplifier.

**IV. BIASING**

In this work we propose using a semi-constant current biasing of all inverters. The inverters used in this design are skewed in size such that even at the fast-slow corner, the nmos trans-conductance is greater than the pmos trans-conductance. The nmos in the unit inverter \((I_U)\) is biased with constant current as shown in Fig. 5(a). The auxiliary inverter \((I_A)\) is used to make the input and output voltage of the unit inverter equal using negative feedback. This is necessary to ensure that the unit inverter nmos is in saturation and also make the cascading of inverters possible. All the auxiliary inverters used in this design are biased with the voltage \( V_{CM} \). This will make sure that all the nmos in these inverters has the same bias current as \( I_{ref} \). With PVT variations the nmos trans-conductance remains constant but the pmos trans-conductance will vary. Since we have designed the pmos trans-conductance to be less than the nmos trans-conductance, the overall trans-conductance variation will be minimal. Any mismatch between the transistors in the biasing network and the forward path will only result in input referred offset due to feedback around the loop.

**V. MEASUREMENTS**

The proposed ADC driver Fig. 5(b) is fabricated in a 65nm CMOS process. The area occupied by the driver is 0.0084 mm\(^2\) out of which 74\% are sampling capacitors. A open-drain pmos (IO device) source-degenerated differential pair is used to drive the output off-chip. Phase and amplitude matched 50\(\Omega\) baluns were used to interface with single-ended equipment. The measurement results are discussed below.

Fig. 6 shows the magnitude response of the ADC driver up to 100MHz. The closed loop gain is 15.66 dB at the Nyquist frequency of 50MHz. The 3dB frequency is 57MHz. The entire ADC driver consumes 2mW of power from a 1V supply. Fig. 7 show the measured IIP\(_3\) of the driver with input tones at 49MHz and 50MHz. An OIP\(_3\) of 40dBm is achieved in the design and the output follows the OIP\(_3\) extrapolation lines even for a rail-to-rail output swing.

Fig. 8 shows the intermodulation distortion (IMD) across the input frequency for three different chips. The IMD for the full rail-to-rail swing is –67dB and varies to –60 dB across 10 chips. The temperature dependence of IMD is shown.

**Fig. 5:** Biasing network schematic (a) and chip micrograph (b)

**Fig. 6:** Magnitude response of the ADC Driver

**Fig. 7:** Measured IIP\(_3\) at 50MHz using two tones with 1MHz offset

**Fig. 8:** Measured IMD for 2V_{pp-diff} output with 1MHz tones separation. Red, blue and green colors shows three different chips
in Fig. 9. At the Nyquist frequency the IMD varies by only 4dB over 80 °C due to the semi-constant current biasing of the inverters and the fact that all blocks in the design are multiples of the unit bias inverter. Fig. 10 shows the intermodulation distortion at the Nyquist rate for rail to rail output swing across 10 chips. Fig. 11 shows a screen capture of a particular test result for two-tone inputs at 49 and 50MHz. Fig. 2 show a screen capture of the noise measurement up to 50MHz for the 100MS/s output. We get a uniform noise floor because of aliasing of out of band noise. The buffer used in the noise measurement has the attenuation of 7dB and hence the actual noise floor is at −124dBm. The total integrated output noise is 1mV rms resulting in an SNR of about 60dB. Although this work is about an ADC driver with a voltage gain of 8 and a sampler, this design can be thought of as a first-order AAF for comparison purposes and hence we use the filter FOM [6].

Table I summarizes our design and compares it with other published state-of-the-art filters with cutoff frequencies in this range. For a fair comparison, we have divided the area by the order of the filter. We get the best IMD (−65dB) at full rail-to-rail swing sampled at 100MHz. We get the lowest input-referred noise, best output swing and the FOM is comparable with the state of art with a DC gain of 8.

VI. CONCLUSIONS

The proposed architecture is significant because it can bridge the gap between the limited swing provided by circuits preceding ADCs and the power and noise advantages provided to ADCs in scaled technologies by full scale input swings. This work achieves the best output swing to VDD ratio at lower power supplies with a linearity (IMD) of 65 dB at Nyquist rate with comparable figure of merit (35aJ) and having a DC gain of 8. Semi-constant biasing scheme reduces the PVT variation. The intermodulation distortion variation across 10 chips is 6dB and 4dB across a temperature variation of 120 °C.

REFERENCES