DC-DC Converter Design

Section:2 – Step By Step Design

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Agenda

1. Motivation
2. Recap
3. Loss mechanisms
4. Design example
   1. Step down with TANK
      1. Design and simulations
   2. Step down NO-TANK
      1. Design and simulations
5. Conclusion
1. Motivation
Source of Power

- Battery voltage changes wrt time
- Different voltage requirements

Graph showing:

- Voltage (V) vs. % Capacity for Li-Ion battery
- After DC-DC Conversion, voltage levels for different applications:
  - PA + Display driver: 2 V
  - Application SOC: 1.5 V
  - Motion processor: 0.5 V

Diagram of power components:
- Li-ion Battery
- Power IC-1
- PA + FBARs
- RF RX/TX
- Motion processor
- Power IC-2
- LTE Processor
- NAND Flash
- Touch Controller
- Wi-fi/NFC
- Audio Codec
- Application SOC

Legend:
- PA: Power Amplifier
**DVFS (Dynamic Voltage Frequency Scaling)**

\[ P_{\text{Digital}} = CV_{\text{DD}}^2 f \]

\[ f = \frac{I}{CV_{\text{DD}}} \]

\[ I = K(V_{\text{DD}} - V_{\text{TH}})^{1\sim2} \]

\[ P_{\text{Digital}} \propto V_{\text{DD}}^{2\sim3} \]
Quick Recap

- Capacitive converter very similarly to linear converter
- They can be modeled by a transformer model

\[ I_{\text{MAX}} = \frac{V_{\text{MAX}}}{R_b} \]

\[ \eta = \frac{V_o}{V_{\text{MAX}}} \]

\[ R_b = \frac{1}{m} \cdot \frac{1}{C_b \cdot F_c} \]
4. Energy Loss Mechanisms
Where does energy go?

- What all we covered?
  - Conduction loss
  - Parasitic loss

- Now we will cover ..
  - Switch Gate Drive (GD) losses
  - Biasing losses
  - Control losses/Digital switching losses
Conduction Loss in SC Converter

- This is due resistive loss across $R_b$
- Fundamental to capacitor charging
- Fixes upper limit of efficiency

\[
\text{Loss} = I_o \left( V_o - KV_{in} \right) = (\Delta V) I_o
\]

\[
\text{Loss} = \frac{(\Delta V)^2}{R_b}
\]
Parasitic Loss

- Integrated caps have top plate/bottom parasitic
- Last session we saw this model

\[ R = \frac{1}{\varepsilon^2 C_f} \]

\[ \Phi_1 \Phi_2 \]

\[ N = 2 \; ; \; K = 2 \]
\[
Loss = A.n.(C_{\text{switch}}) \cdot f_{\text{sw}} \cdot V_{\text{sw}}^2
\]

\[
A = \text{Sizing} \cdot n = \# \text{ switches}
\]

\[
\text{Sizing}_{\infty} = 1 + \frac{1}{3} + \frac{1}{9} + \frac{1}{27} + \ldots = 1.5
\]

But we choose finite stages so choose, \( A = 1.4 \)

- \( C_{\text{sw}} \) is related to \( C_b \)
- \( V_{\text{sw}} \) is related to \( V_{\text{in}} \)

- In reality GD loss is similar to conduction loss!
Types of Passives

- **MOS:**
  - Highest parasitic
  - High leakage
  - Highest density

- **MOM:**
  - High density
  - Low leakage
  - Low parasitic

- **MIM:**
  - Lowest density
  - Lowest parasitic
  - Lowest leakage
5. Design Examples

Example 1

Step Down Case
## Example 1: Specifications

<table>
<thead>
<tr>
<th>Desired Specs</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>0.5</td>
</tr>
<tr>
<td>Output current (mA)</td>
<td>1</td>
</tr>
<tr>
<td>Peak output ripple (%)</td>
<td>&lt;=5</td>
</tr>
<tr>
<td>Tank cap (pF)</td>
<td>250 (Given)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tech. Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor density</td>
<td>4fF/um²</td>
</tr>
<tr>
<td>Bottom plate parasitic</td>
<td>2%</td>
</tr>
<tr>
<td>Switch resistance</td>
<td>150 ohms/um</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>2fF/um</td>
</tr>
</tbody>
</table>
Aim Of Example

- Converting specs to design
- Design simple open loop converter
- Understanding capacitance and frequency tradeoff.
- Using framework for device sizing
- Use open loop as point solution for closed loop
Design Variables

- **Dynamic operating variables**
  - Switching frequency, $f$
  - Switching (bucket) capacitance, $C_{\text{bucket}}$

- **Fixed variables**
  - Switch sizes
  - Filter capacitors
Design Steps

- **Step 1**: Choose type
  - Buck, boost or negative
  - This case
    - BUCK (step-down)

- **Step 2**: Choose conversion gain (k:1)
  - \( k \sim \left[ \frac{V_{in}}{V_{out}} \right] \); In this case \( k = 2 \)
  - IPO-OPG

We recall
### Design Steps

- **Step 3**: Finding optimum output voltage

\[
\eta = \left[ \frac{1}{2} + \frac{1}{2} \left( \frac{1 - \frac{\varepsilon_2 V_o}{2(V_{max} - V_o)}}{1 + \frac{\varepsilon_1 (V_i - V_o)}{2(V_{max} - V_o)} + \frac{\varepsilon_2 V_o}{2(V_{max} - V_o)}} \right) \right] \left( \frac{V_o}{V_{max}} \right)
\]

- Using \( \varepsilon_2 = 0.02 \) and \( \varepsilon_1 = 0 \) we get:
  - \( \eta = 80.43\% \)

- Capacitor parasitics set the optimum operating voltage
**Design Steps**

- **Step 4**: Output impedance
  - $I_{out} = 4(0.05)C.f$
  - $C.f = 5 \text{m Ohm}^{-1}$
  - We have fixed $C.f$ value

- **Step 5**: Sizing of MOS devices/switches
  - $4(2 \times RC) = \frac{T}{2} = \frac{1}{2f} \{4\tau \text{ settling}\}$
  - $R = \frac{1}{16.C.f} \sim 12 \text{ Ohms}$
  - Using technology parameter; $R = 16\mu/60n$
Till Now

Buck → 2:1 (IPO-OPG) → Vmax-Vo

Efficiency = 80.43
Design Steps

- **Step6**: C-F trade off
  - Ripple = |±ΔV| = \( \frac{I}{2fC_{tank}} \)
  - \( F = 200 \text{MHZ} \)
  - \( C_{\text{bucket}} = 25 \text{pF} \)

- **Step7**: Verification of assumptions
  - \( C_{\text{bucket}} < 0.1 \ C_{\text{tank}} \)
    - 25pF < 0.1 x 500pF
  - 4RC_{\text{bucket}} \leq T/2
**Step8**: Gate drives losses

- Depends on switches
- Use a scaling factor = 1.4
- Each switch gate cap
  - \(2 \text{fF} \times 16 = 32 \text{fF}\)
- Gate drive loss
  - \(1.4 \times (1.2)^2 \times 32 \text{fF} \times 200\text{MHz}\)
  - \(13\text{uW}\)
- Efficiency loss = 1.9%
## Design Steps

<table>
<thead>
<tr>
<th>Designed results</th>
<th>Values</th>
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<tbody>
<tr>
<td>Efficiency</td>
<td>(80.3-1.9)=78.4 %</td>
</tr>
<tr>
<td>Power density</td>
<td>0.01W/mm$^2$</td>
</tr>
<tr>
<td>Gate drive losses</td>
<td>13 uW</td>
</tr>
<tr>
<td>% of GD</td>
<td>1.9%</td>
</tr>
<tr>
<td>Bucket Cap</td>
<td>25 pF</td>
</tr>
<tr>
<td>Cap area (total)</td>
<td>68750um$^2$</td>
</tr>
<tr>
<td>Switch sizes (W/L)</td>
<td>16u/60n</td>
</tr>
<tr>
<td>Frequency</td>
<td>200MHz</td>
</tr>
</tbody>
</table>
Simulation Test Bench

![Circuit Diagram]

- **Vin**: Input voltage
- **Cbucket**: Capacitor
- **Vout**: Output voltage
- **CTANK**: 250pF
- **1mA**: Current
- **16u/60n**: Capacitance
- **1.2V**: Voltage
- **25pF**: Capacitance
Steady State: \( V_{out} = 500\text{mV}, \, V_{in}=1.2\text{V}, \, I=\text{mA} \)
Ripple: $V_{out} = 500\text{mV}$, $V_{in}=1.2\text{V}$, $I=\text{mA}$

27 mV ripple
Design Summary

- Simple open loop design
- Efficiency = (80.3 - 1.9)% = 78.4%
- $C_{\text{tank}}$ required ($C_{\text{tank}} \gg C_{\text{bucket}}$)
- Almost complete charging ($4\tau'$)
- Low power density
- Switch parasitics neglected
Example 2

No Tank Case
Second Example

- More complete design of previous example
- **No explicit $C_{\text{tank}}$!**

**Aim:**
- No explicit $C_{\text{tank}}$
- Multiple phases
- Use of previous example as point solution

- Complex design tradeoffs
- Not unique design solutions
Multiple Phases I

- N phases -> ripple goes down by N times
- Effectively increases frequency by N
  - Careful implementation
  - Requires lower power
- Each phase sees \( \frac{N-1}{N} C_{\text{bucket}} \) (total) as CTANK
- Area saving -> Increased power density
Multiple Phases II

- More complete design of previous example
- **No explicit $C_{\text{tank}}$ !!**
- **Aim:**
  - No explicit $C_{\text{tank}}$
  - Multiple phases
  - Use of previous example as point solution
- Complex design tradeoffs
- Not unique design solutions
## Example 2: Specifications

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</tr>
<tr>
<td>Output Current (mA)</td>
<td>1</td>
</tr>
<tr>
<td>Output ripple (mV)</td>
<td>10</td>
</tr>
<tr>
<td>$C_{tank}$</td>
<td>0</td>
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**Design Steps**

- **Step 1:** Choose type
  - Buck, boost or negative
  - This case (1.2V to 0.5V)
    - BUCK (step-down)

- **Step 2:** Choose conversion gain (k:1)
  - \( k \sim \left[ \frac{Vin}{Vout} \right] \); In this case \( K = 2 \)

- IPO-OPG
**Design Steps**

- **Step 3**: Finding optimum output voltage

\[
\eta = \left[ \frac{1}{2} + \frac{1}{2} \left( 1 - \frac{\varepsilon_2 V_0}{2(V_{\text{max}} - V_0)} \right) \right] \left( \frac{V_0}{V_{\text{max}}} \right)
\]

- Using \(\varepsilon_2 = 0.02\) and \(\varepsilon_1 = 0\) we get:
  - \(\eta = 80.3\%\)

- Capacitor parasitics set the optimum operating voltage
**Design Steps**

- **Step4**: Output impedance
  - $I_{out} = 4(0.05)C.f$
  - $C.f = 5$ m Ohm$^{-1}$
  - We have fixed $C.f$ value

- **Step5**: Sizing of MOS devices/switches
  - $4(2xRC) = T/2 = (1/2f) \{4\tau \text{ settling}\}$
  - $R = 1/(16.C.f) \sim 12$ Ohms
  - Using technology parameter; $R = 16u/60n$
Design Steps

- **Step 6**: Ripple $\sim \frac{I}{2fC_{bucket}} = 100\text{mV}$

- **Number of phases to be decided**
  - We choose $N = 9$ (Easier!)
  - Effective ripple $= 100/9 = 11.11\text{ mV}$
  - 9 phases are produced by ring oscillator, $N=9$
  - Extra power is independent of $N$
    - $P = NCV^2f = N\left(\frac{1}{2N\tau}\right)CV^2$
    - Current starved are best suited
Design Steps

- **Step 7:**
  - Also no of phases can affect efficiency *

*Ripple loss*

\[
P_{L-tot} \approx \left( V_{min} + \frac{\Delta V}{2} \right) \left( I_L + \frac{1}{k_{interleave}} \cdot \frac{\Delta I}{2} \right)
\]

This case!
N=9 chosen

* LE et al.: DESIGN TECHNIQUES FOR FULLY INTEGRATED SWITCHED-CAPACITOR DC-DC CONVERTERS, JSSCC 2011
Switch Parasitic

**Step 8:** Switch parasitic should not contribute to bucket parasitic

\[
C_{bucket} = 1000 \left( C_{switch, S} \right)
\]

\[
\left( C_{switch, S} \right) = 16 \text{ fF}
\]

\[
C_{bucket} = 16 \text{ pF} \Rightarrow f = \frac{5 \text{ m}}{16 \text{ pF}} = 312 \text{ MHz}
\]
Design Steps

- **Step9**: Gate drives losses
  - Depends on switches
  - Use a scaling factor = 1.4
  - Each switch gate cap
    - \(2fF \times 16 = 32fF\)
  - Gate drive loss
    - \(1.4 \times (1.2)^2 \times 32fF \times 312MHz\)
    - 20.13 uW
  - Efficiency loss = 2.1%
Simulations

OUTPUT voltage (Steady state)

Ripple = 50 mV

9 Multiple phases
Design Summary

- Zero explicit C_{tank}
- Efficiency = 78.2\%
- Higher power density
- Almost complete charging (4\tau')
- Switch parasitics contribution cannot be neglected and help to break C.f product
- Multiple phases were used
Design Flowchart

Buck/Boost/Negative

Decide K

Decide conduction efficiency

Parasitic efficiency

Switch sizing

C_{tank}

Ripple

C/F decision

Gate drive losses

NO C_{tank}

Multiple phases

Switch parasitic

Gate drive losses
Conclusions I

- Efficiency is important
- But power density is important too.
- FOM = Efficiency × Power density

ISSCC 2014 capacitive converter trends
Conclusions II

- Unified framework followed for circuit design
- Two circuit examples
  - Simple procedural example
  - Complex sequential example
- \( C_{\text{tank}} \rightarrow \) easy \( \rightarrow \) Less power density
- NO \( C_{\text{tank}} \rightarrow \) complex \( \rightarrow \) higher power density
- Design flow chart developed
- Multiple phases give low ripple
Thank you